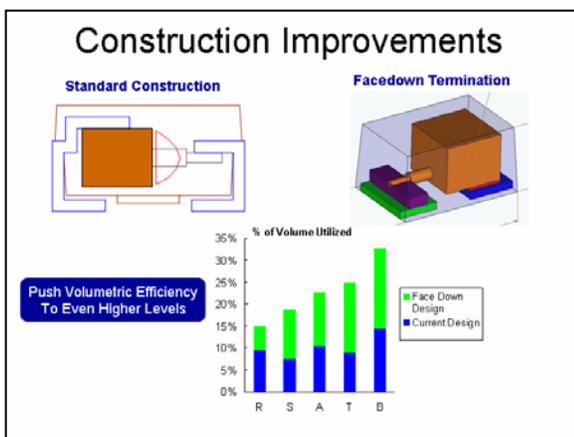


KEMET Electronics Corp.

Lower, Thinner SMT Polymer Capacitors

The world is moving to lighter, smaller, or thinner devices. The development and alteration of the components used in these devices is following this trend with thinner packages being presented for these assemblies, including the tantalum, aluminum, and polymer based capacitors. The present designs are centered on achieving a thickness or chip height approaching 1 mm. The ideal package is very thin, small in footprint, and high in capacitance.

Ceramic MLC capacitors have traditionally led the way to miniaturization and this is readily observed in the offering of chips down to the 01005 size (0.25 x 0.13 mm); but the capacitances obtainable in these miniature packages are also fairly small. Recent MLC capacitance extensions achieved through thicker chips have been concentrated in the larger chip arena resulting in some chips with thicknesses close to 3 mm for 6.3 VDC chips. Moving the thickness lower through thinner dielectrics and electrodes may be achievable at some time in the future, but not today. Also, the MLC package has a wrap-around termination on the chip ends that adheres to the solder pads on the board; but this wrap-around also creates a termination exposed on the top face of the chip, thereby requiring a space above the chip to be clear of any metallic contact that could create a short here.



The illustration on the left ("Construction Improvements") highlights the loss of efficiency of the tantalum-based capacitor moving to smaller packages. The "A", and "B" represent EIA specified chip structures, the "R" represents a package similar to an 0805 chip, and the "S" and "T" represent lower profile or thinner chips in the same footprints as the "A" and "B", respectively. Looking at the bar graph of the percentage of volume utilized, the range for the current or traditional designs varies between 7 and 13 percent. Looking at the "Standard Construction" drawing, the actual capacitor portion of the structure is the solid rectangle (orange-brown), while the remaining volume is used for the interconnections and leadframe.

The "Facedown Termination" drawing in the illustration shows a radical departure from the traditional design. The block of tantalum bearing capacitive structure can now take up a greater percentage of the package. Again, referring to the bar graph, the efficiency increase

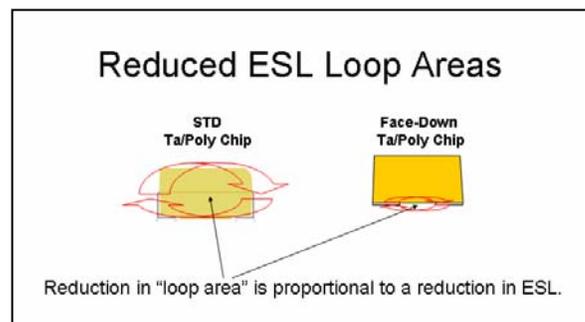
is more than double for some of these cases.

The new products that will take advantage of this facedown termination design will be led by the "T" case offering of a tantalum-polymer (KO) design. It will be offered with a maximum height of 1.2 mm. Though this presentation has concentrated on smaller footprint, the demand for more capacitance pushes the thinner requirements into larger case sizes. The second offering will be a larger chip (7343 footprint as in traditional "D" case), in response to the higher capacitance required for many processor applications, but at a height of 1.7 mm ("Z" Case). Designs for 1.5 and 1.0 mm are also being pursued across all chip sizes.

In some cases, the chips will be designed to fit the traditional solder pads of the standard chips, but there will be room for optimizing these pads that will allow for reduced area. Consider that with the facedown termination no vertical element of a lead is presented - eliminating the variations of the solder fillet along the surfaces of these vertical structures (and reducing the pad area).

Additionally, by eliminating the vertical element of the leadframe, outside the plastic package, the current path is dramatically reduced. The effective reduction in the current loop cross sectional area corresponds to a significant reduction in ESL. The "T" case has nearly a 50% reduction in ESL, while the larger 7343 chip will have an ESL near 0.4 nH (nearly a 75% reduction).

To get the latest chip offerings and plans for lower ESR/ESL capacitors, visit the KEMET web site at www.kemet.com, or contact our sales office.



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