# KEMET Spice – An Update

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### *Abstract*

*The frequency response of capacitors is related to complex relationships of the capacitance as well as the parasitic resistive and inductive elements of this device. In 1995, KEMET presented a Spice capability [1] for the SMT capacitors as worksheets that were run in Mathcad® [2]. Today this capability is available as a Windows based software with relationships defined for not only frequency, but also for application variations of temperature and bias conditions. We will define the methodology in the correlation of the complex response for aluminum-polymer, tantalum ($MnO_2$ and polymer), as well as ceramic SMD chip capacitors. This update will also explore the relationship of the designs to inductance and power dissipation or ripple current capabilities.*

## Limitations of Mathcad®

It was difficult to design the worksheets because the response calculations were based on a single model with certain seed values that were dependent on the specific part type requested. Some of these seed values would be consistent for a family or case size, but would vary with the specific values found within that group. The support files for these models were initially limited to numeric values stored as a matrix, with no correlation to an alpha detailed description of the part number.

The worksheets were divided by case size and style for tantalum, and chip size, dielectric and voltage for the ceramics.

This software also has a penchant for constant updates with no legacy maintained. Any worksheets created in an earlier version are immediately upgraded to the latest version when saving any changes. Any worksheet edited in the newer versions, became inoperable in the earlier versions. Additionally, an attempt to secure some sort of discount coupons for any of our customers that would need to purchase the software was denied by Mathcad®.

## Windows® compatible – KEMET Spice

The calculations were converted to Visual Basic routines that allowed full duplication of the Mathcad® worksheets with the full Windows® [3] adaptability of the graphics interface existing (e.g., alpha character creation and disassembly of the part numbers, pull-down menus, hot-keys, etc.).

Compatibility was only an issue when the operating system changed for 16-bit to 32-bit. The program could have continued to be sourced as a 16-bit version, but support for the older programming languages is always a tenuous predicament. For a while, both 16 and 32-bit versions were offered, but today only, the 32-bit version is being supported. We may come to these issues when 64-bit dominance begins, but that's a future problem.

The software is available for download from our web site (www.kemet.com as in Figure 1). An instructional manual for the software is also available. We suggest downloading the manual because some capabilities of this software might not be readily apparent to all (exporting data and models, hot-key shortcuts, etc.)


***Figure 1. Download KEMET Spice from web page.***

## The program

The basic models created in the Mathcad worksheets have been recreated in the KEMET Spice [4] program. Over the years, some enhancements have been added, and we will attempt to cover the major changes that have taken place. A review of the specific changes created with each revision is available through the help screen index.

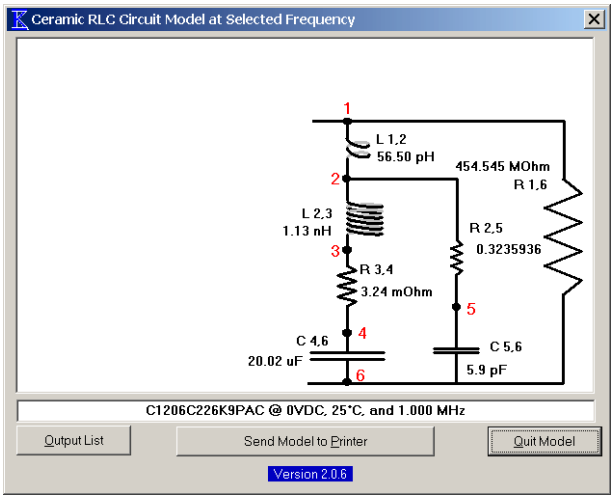


***Figure 2. Ceramic RLC model.***

The program combines all of the initial 50 worksheets dealing with SMT chips, from Mathcad, into a single program.

## The ceramic model

The model used to calculate the response for a ceramic capacitor is a variation of the simple RLC model (Figure 2). The response of the model is targeted to mimic the measured response of a specific chip. The distinguishing feature in this software is that the ESR ($R_{3,4}$) is factored by frequency, as is the main body of capacitance ($C_{4,6}$). The inductance is factored by the structure of the MLC and is related to the number of plates required to achieve the capacitance. We use the inductance (ESL) as derived from the self-resonance of the measured response. In the model the ESL is divided 95% to 5% as $L_{2,3}$ and $L_{1,2}$, respectively, to prevent the secondary or parallel resonance from creating a point where impedance is decreasing after the parallel resonance (another series resonance is created immediately after, to show increasing impedance (Z) with increasing frequency). Some models use the inductance as measured well above self-resonance, but these two inductances are rarely equal. In the future, we will include the change of inductance as it decreases from the self-resonant point to that frequency well above this point.

The capacitance and ESR are also factored by the DC bias voltage, and we have included this response in the model (operator can change the DC bias to see the effects). For the higher capacitance packages for low voltage, these two parameters are also factored by the AC signal, and this is another factor that will be included at some time in the future.

### *Correlation to measured response*

When we run the frequency scans, we normally run at least 5 pieces each time. The actual fit is targeted for the average response of these five, or in the case of wide disparity, the 3rd Quartile of the range defines the targeted response.

The parallel elements $C_{5,6}$ and $R_{2,5}$ create a parallel capacitance effect through the termination faces of the chip, and are responsible for the parallel or secondary resonance. $R_{1,6}$ represents the insulation resistance of the capacitor, and has little impact on the frequency response of the chips.

The capacitance and resistance dependence on temperature is also included, and is dependent on the type of dielectric utilized in the structure.

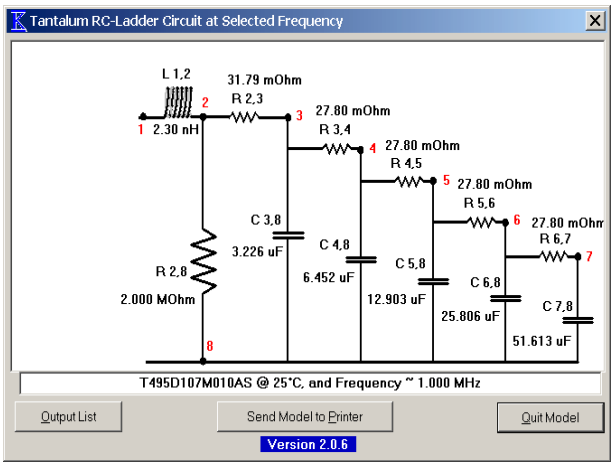


***Figure 3. Electrolytic (Al/Ta) model.***

These models have a capability of creating an ASCII file with a net list output of the elements within them.

## The electrolytic model

This model (Figure 3) is more complex than the ceramic model. These devices exhibit a capacitance loss with increasing frequency that can be mimicked by an RC-Ladder circuit ($C_3$ through $C_7$ and $R_2$ through $R_6$). This portion contains resistive values that are nearly identical, with capacitance elements that are increasing in magnitude as the progression into the circuit moves to the right. This configuration allows the simplest but closest duplication of the observed capacitance decay with frequency we observe.

Unlike the ceramic model, there is no capacitance change associated with AC or DC bias, but there is a change of capacitance and ESR with temperature. These changes for the aluminum and tantalum are considered to be equal (linear change from 0% at +25°C to -15% at -55°C, and from 0% at +25°C to +15% at +105°C). The resistive elements, $R_3$ through $R_6$, are also factored as having a negative temperature coefficient of resistance (TCR); but this is true only for the $MnO_2$ devices (tantalum T4xx and T510 series).

As the ESR's become appreciably lower for the polymer devices (T52x, T53x, and A7xx), the decay in resistivity for the semiconductor elements (negative TCR) is balanced by the positive TCR of the metal or conductive elements of the structure. We have measured some devices where the resistivity decreases slightly (negative TCR), some with no appreciable

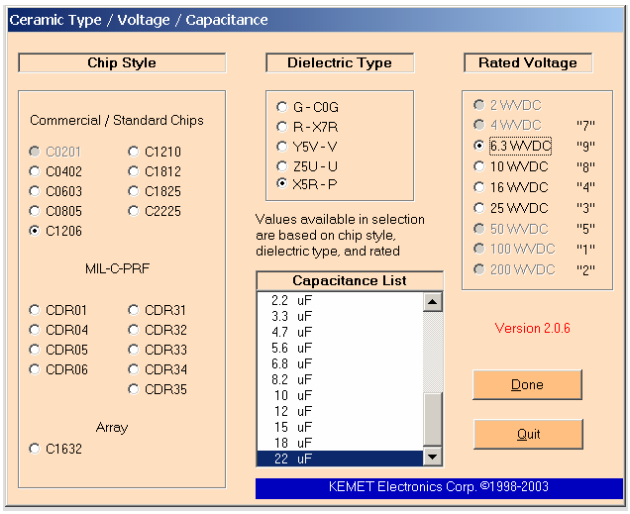


***Figure 4. MLC selection form.***

change, and some have resistivity increases (positive TCR). Once these observations were made, then the resistivity calculations for the step resistors included a portion with a positive TCR (+0.4%/°C), and a portion of negative TCR.

In this model, the resistive elements are also factored by frequency. This effect was detailed in the earlier paper presented and the factors (upper and lower frequency nodes) are device dependent, down to the capacitance and voltage of the device. These factors are adjusted to get the calculated response to fit the measured response.

## Selecting the capacitor

The program allows the operator to choose between ceramic and electrolytic capacitor forms. The ceramic form lists the chip sizes, the dielectrics, and the voltages available. Once these are selected, specific capacitance values within those constraints are listed, and the operator then selects the value.

The chip styles encompass the standard SMT offerings as well as MIL-C-PRF designators, and the array product. Soon to be added will be the large ceramic chip products picked up from the Sierra-KD purchase by KEMET.

Selecting any chip style will define the offerings within the dielectric type. Selecting the dielectric type will define the voltage offerings, and selecting any of the voltage offerings will then dictate the capacitance values available for these selections. Selecting a capacitance value and clicking "Done" normally moves the display into the plotted response of impedance and ESR versus frequency.

If a military part number is selected, then the operator can then be more specific as to the finer details (termination, tolerance, failure rate, etc.) but none of these selections will affect the frequency response. Previously the program would show the part number created and allow selection of different tolerance, but this feature was found to be of little value. It can still be accessed by pressing the escape key <Esc>. This key will back up one screen at a time, and if selected when the plot is shown, a detailed selection for the part number can be viewed and changed. Again, these selections have no impact on the plotted response.

For the tantalum, the number of selections is paired down somewhat as no dielectric is selectable (though choosing between a tantalum and aluminum chip does dictate two different dielectrics). The chip style or family is selected initially. The selections here are broken down into these categories: Commercial or Standard T491, (& T494); Low Profile (commercial) Chips ('R' through 'V' case); then the low-ESR, T495 family; the fused T496 family; the tantalum-polymer (T52x, T530); and finally at the bottom is the aluminum-polymer (A7xx).

Selecting the chip style defines the voltage choices, and selecting a voltage rating then defines the capacitance available. Some part types will have a 4-character code defining some special characteristic for that part, and these codes will be explained immediately below the window of available capacitance. In the illustration of Figure 5, the 4-character suffix defines the maximum

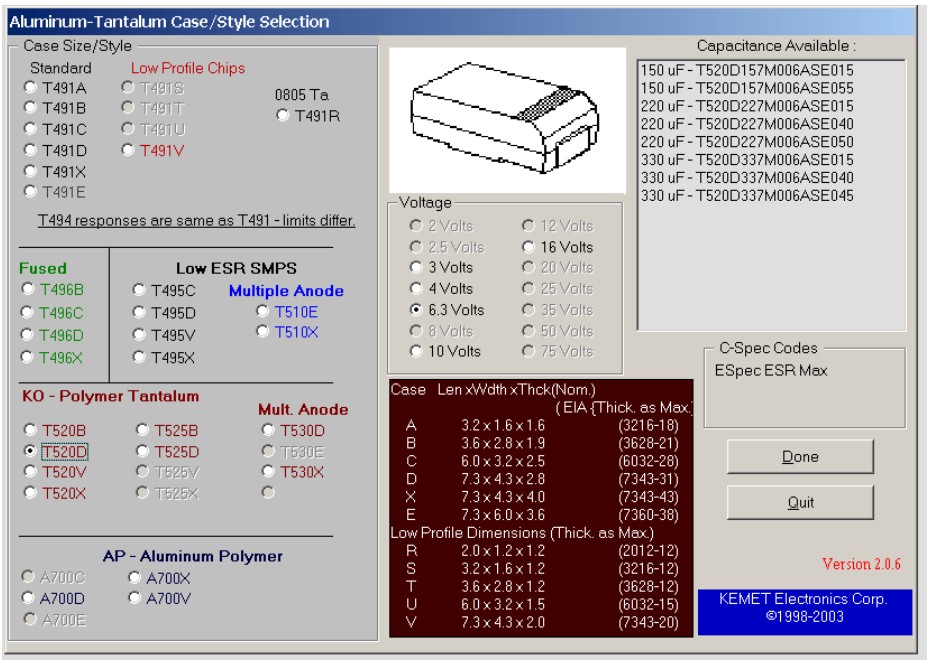


***Figure 5. Electrolytic capacitor selection form.***

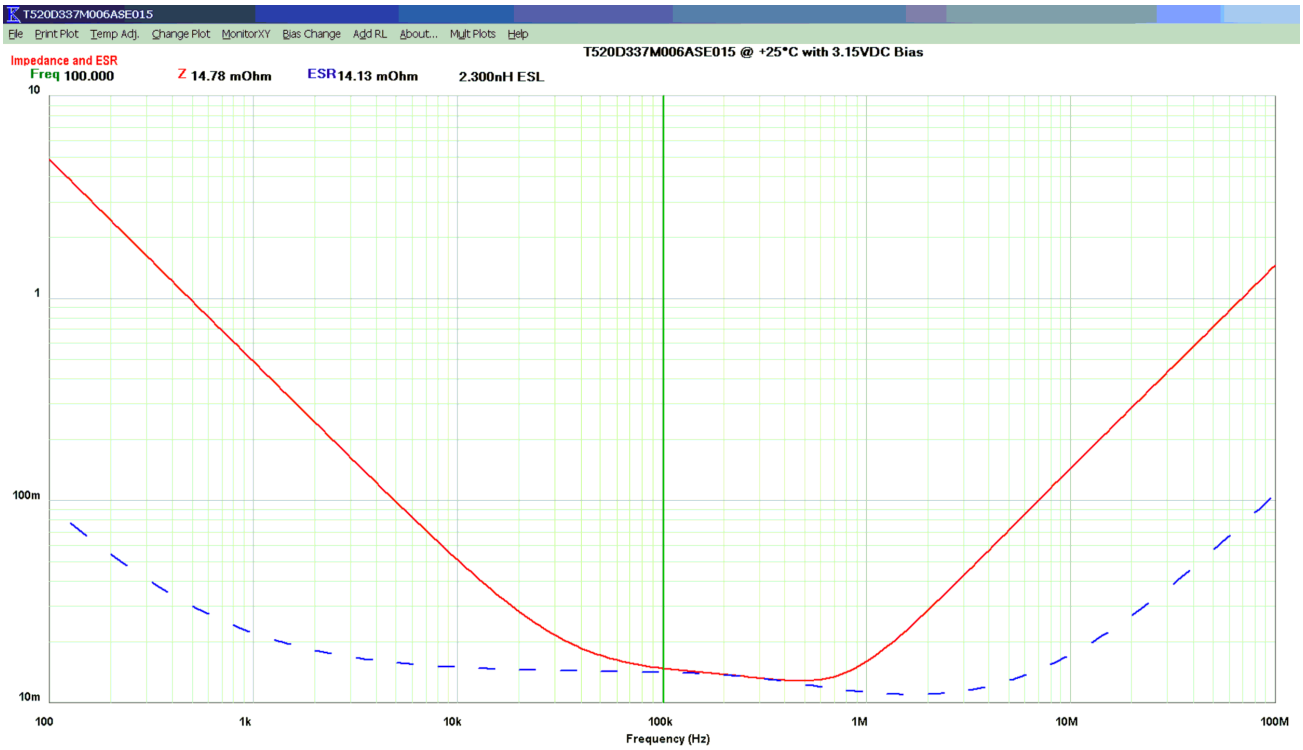


***Figure 6. Plotted response of impedance and resistance versus frequency (Hz).***

ESR at 100 kHz, and +25°C, for each device.

Once the operator selects a specific part type (with capacitance), the program will move on to the displayed plot after "Done" is selected.

## The displayed response – Z & ESR

The program actually calculates the frequency, temperature, and bias (if any) related parameters for each frequency. There are 50 divisions of each decade (equal distance on log scale) used to define the frequency points. Once these are set, the program then calculates and plots the resulting impedance and resistance at each of these frequencies.

The frequency range can be manipulated for each plot, and the default range can be changed by the operator. The vertical range (ohms as shown in Figure 6) is determined by the range of response and cannot be changed by the operator.

A scroll line (shown in Figure 6 as a green line at 100 kHz) can be moved with the mouse and the positional values are detailed along the top of the plot (the **Freq**uency as **100.000 kHz**, **Z** as **15.39 mOhm**, and the **ESR** as **13.99 mOhm**).

The part type, ambient temperature, and DC bias are revealed in the center, above the plotted area. The program defaults the DC bias to one-half of the rated voltage for the electrolytics as this will allow the largest possible peak-to-peak ripple without exceeding the rated or going negative (below 0 VDC). For MLC capacitors, the default DC bias is set to 0 VDC, again allowing the highest peak-to-peak response where possible.

There are pull-down menus along the top of the screen and among these menus are:

**File:**
- Instructs how to copy screen to clipboard ● Export data to ASCII File ● Start over ● Choose another ● Choose another (MLC or electrolytic – part dependent) ● Exit program

**Print Plot**
- Print Z/R ● Print C/L ● Print I/V ● Print All Freq ● Print *dv/dt* ● Print Cap/*dt* ● Print All Time ● Print All Freq/Time ● Printer Setup

**Change plot**
- Plot Z/R ● Plot C/L ● Plot I/V ● Plot dv/dt ● Plot C/dt ● Change Freq Range ● Grid Lines

**Temp Adj**
- +105ºC (part dependent) ● +25ºC ● -55ºC ● Custom ● Power Rise ºC

**About**
- Program ● SPICE ● Temp Note ● Bias Note ● ESL Explanation

**Mult Plots**
- Add Plot ● Del Plot (only if multiple active)

**Help**
- Contents, Index ● Impedance & ESR ● Capacitance & Inductance ● RMS Current Voltage ● Help on 'Graph' (screen dependent)

There are hot-keys to quickly access some of these menu items (e.g., Ctrl+H = highest temperature as ambient, Ctrl+R = +25ºC as ambient, Ctrl+L = lowest tem-

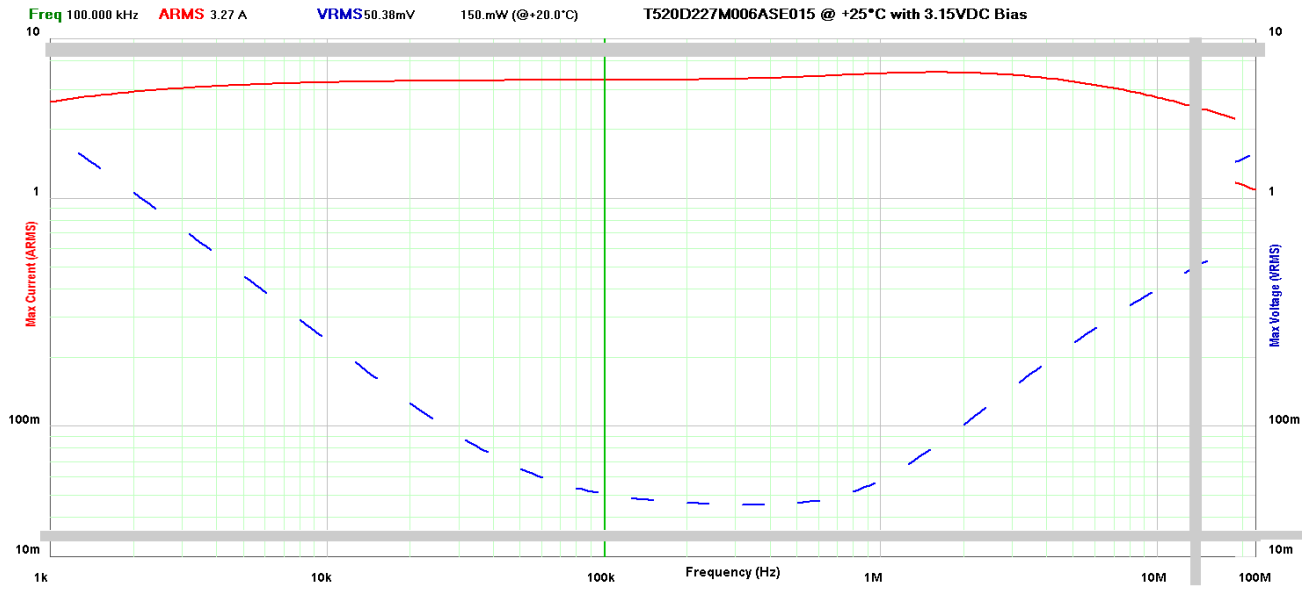


***Figure 7. RMS Current & Voltage (truncated) versus frequency (Hz) .***

perature [-55ºC] as ambient, Ctrl+T = allow operator to enter any temperature).

## Other Plots

Plots of RMS current and RMS voltage versus frequency show the maximum allowable signal at any one frequency. In Figure 7, the plot is shown with the red line defining the RMS current and the blue line defining the RMS voltage.

Along with the monitored frequency (100 kHz), ARMS (3.27 A), and VRMS (50.38 mV) display is the power rating and the temperature rise that defines the limiting factor. The operator can change the allowable temperature rise. For the sake of conformity, the default is +20ºC, but as long as the rise plus the ambient does not exceed the maximum, the operator may enter any allowable delta.

A plot of capacitance versus frequency details the capacitance change experienced with the electrolytic devices. The plot shown in Figure 8 shows this decay for a T491 device. The part measures 330 µF at 120 Hz, as it is measured per specification. Yet at 100 kHz, the capacitance has dropped to 40 µF.

After the part goes into self-resonance (near 1 MHz), the inductance is then plotted (the beginning of the blue line). Because the temperature has such a huge influence on the resistive elements in the RC-Ladder network for this device, at - 55ºC the capacitance drops to 22 µF

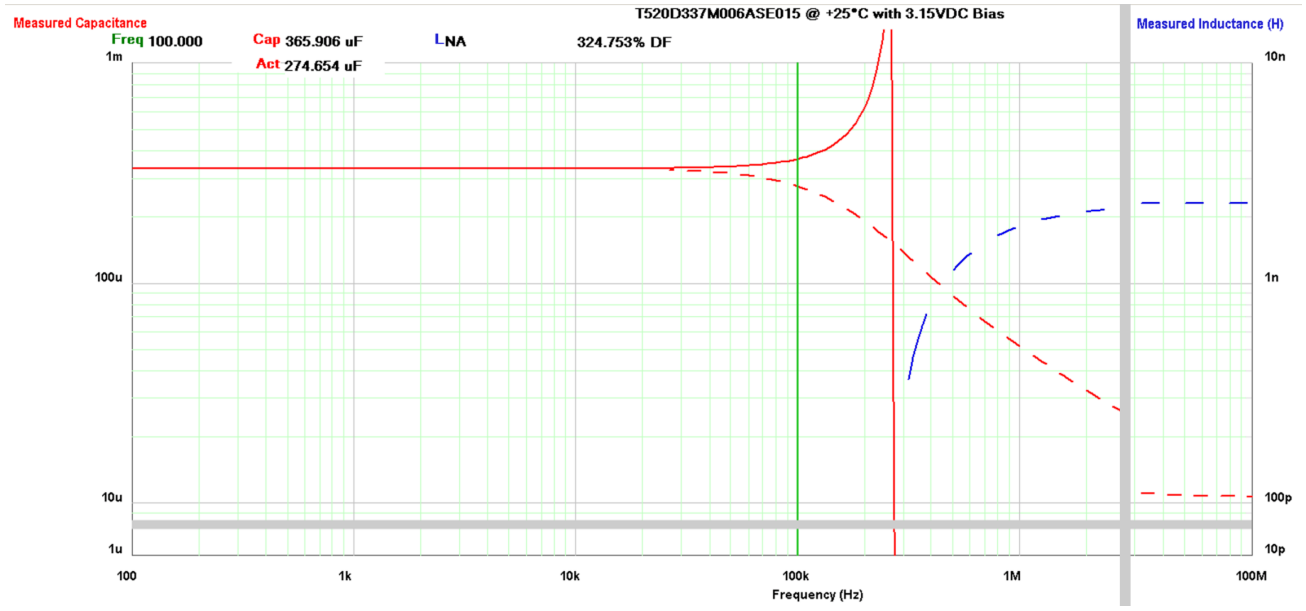


***Figure 8. Capacitance drop with frequency for T491 device.***

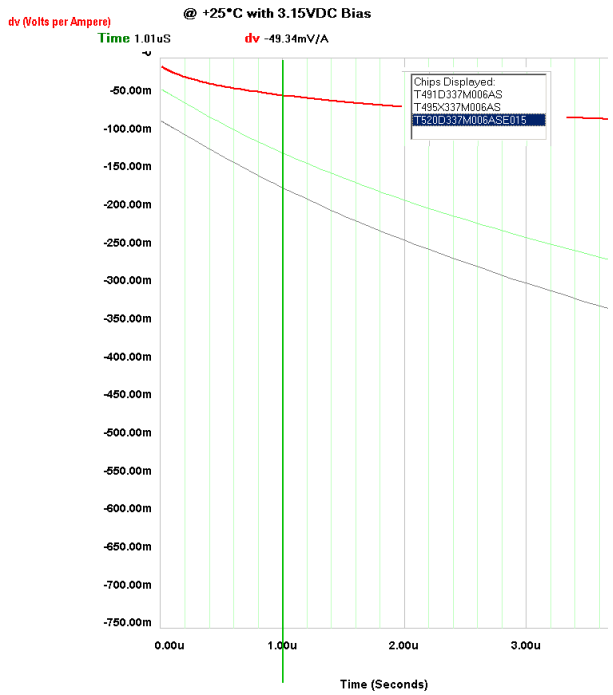


***Figure 9. Plot of dv/dt responses (dv-per-Ampere).***

at 100 kHz, and rises to 56 µF at +85ºC.

In addition to the frequency plots, two time-related plots are included. Shown in Figure 9 is a portion of the *dv* versus Time (seconds). The *dv* is just that voltage related to capacitance and resistance as the inductive voltage includes another independent variable (*di*/*dt*). The following relationship defines this voltage. The voltage is negative as the capacitor is discharging,

$$dv_t = \sum_{0}^{t}\left(\frac{i}{C_t}\times dt_t\right)+(i\times ESR_t)$$

***Formula 1. dv/dt calculation.***

## Multiple plots

Side-by-side comparison of the printed plots is eliminated with the ability to show multiple plots on a single graph. The multiples can number between two and five, allowing five different pieces to be viewed, or one piece at five different temperatures, or one piece at five different DC bias conditions.

In Figure 9, three different pieces are shown in the *dv*/*dt* plot. The monitored points are shown for the dark red trace (T520D337M006ASE015, with -49 mV/A at 1.01 µS), and the operator can scroll through the different traces by using the <Cursor-Up>, and <Cursor-Down> keys. The specific part highlighted is shown in a box in the upper-right corner of the plot. The other pieces (T495 and T491) show increasing dv/dt compared to the T520 part.

Multiple views of the same piece for various temperatures or for various DC biases can be utilized with this feature.

| Case | Power (mW) | °C/W |
|---|---|---|
| A | 75 | 3.75 |
| B | 80 | 4.00 |
| C | 110 | 5.50 |
| D | 150 | 7.50 |
| X | 165 | 8.25 |

***Table 1. Power and thermal resistance vs. chip size.***

## Voltage derating

Unique to electrolytic capacitors is the "derating" of the voltage rating at elevated temperatures. For tantalum capacitors, this effect allows the rated voltage of the capacitor to be the same from -55°C through +85°C. Above +85°C through +125°C, the voltage rating is decreased from 100% of the initial rating at +85°C, to 67% of the initial rating at +125°C. The voltage rating for devices between these temperatures is considered to be a linear interpolation of the voltage defined by these two points. At +105°C, approximately halfway between the two points, the voltage rating is considered to be 80% of the initial rating (83% by calculation).

The program automatically compensates the voltage rating for temperature. If the applied DC bias is above this derating as the operator changes temperature or DC bias, an audio and visual alert is supplied to warn of this condition.

## Power Rating – Tantalum

The power capability of the tantalum chip is fairly straight forward as these ratings are typically included in the manufacturers' catalogs. This rating normally reflects the wattage that will create an *acceptable* temperature rise. Though this temperature rise is normally specified as +20°C, it is usually slightly below this as a margin of safety. The ratings will change as the case size changes, with larger cases having greater power ratings.

The structure of the tantalum chip may be viewed as a pellet within a plastic package, connected to a leadframe for an external connection. The heat generated within the component can travel through the case and flows off the surface of the chip, or it can flow along the metal connections, the same as the electrical path. In fact, the path through the case plastic is very restrictive as the plastic is a thermally insulative material, and the majority of the heat out of this package is through the metal structure. Because the pellet size varies little as the capacitance and voltage ratings change for each case, this path's dimensions are fairly constant. As such, the thermal transfer capability is fairly consistent, and determined by case. If we look at the power rating

of the case and consider that these ratings are realized with a +20°C temperature rise, then we can take that power rating, divide by 20, and yield the thermal resistance rating of the device, as is listed in Table 1.

Only a major change in the structure of the tantalum chip will change the power capability of that chip. An example of this is that for the multiple-anode structures of the T510 or T530 'X' case, the power dissipation rises to 270 mW, as three pellets are in parallel in these chip packages.

## Power Rating – Ceramics

The thermal dissipation in a ceramic chip also has two possible paths: radiated through the ceramic body, and conducted through the electrode plate system. As with the plastic package of the tantalum, the ceramic dielectric is not a good thermal conductor, instead it is a good insulator. The electrode plates are very good conductors, and in this package carry most of the heat out of the package.

For a given dielectric type, chip size, and voltage rating, the variation of capacitance is created with a variation of electrode count. This leads to an increasing thermal transfer capability as the number of electrodes increase for the higher capacitance values.

A good description of the thermal modeling and calculations is given in a paper, "*Ceramic and Porcelain Multilayer Capacitors – Thermal Resistance, Power Dissipation and Current Rating,*" by Schabauer and Blumkin, of ATC Ceramics [5]. The model divides the capacitor in half, assumes a consistent temperature in a plane at this point, and looks at the parallel thermal conduction paths created by the electrode and dielectric configurations.

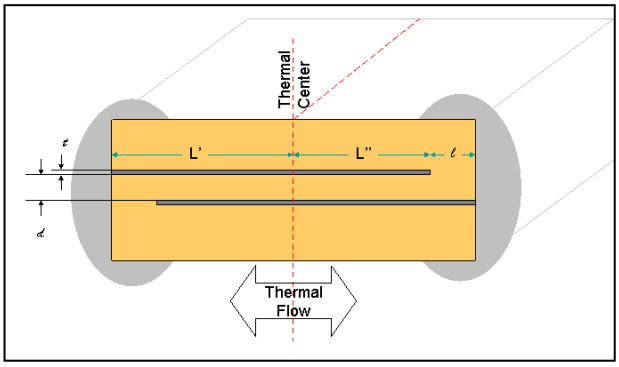


***Figure 10. Thermal paths for MLC chip.***

From the center plane (thermal center), there are three possible thermal paths. The first is from this plane through the electrodes (L') which are terminated at each end of the chip. A second path flows in the opposite direction in these electrodes (L''), towards the ends of the chips, then through a small segment ($\ell$) of the dielectric. The third path has the heat flowing from this plane, through the dielectric to the termination ends of the chip.

These paths have physical constraints and material properties that allow a calculation of each thermally resistive path, and the combined parallel effects for each design. The calculations result in a combined thermal resistivity factor defined in watts per degrees Celsius. Using this figure and multiplying by an industry quasi-standard of +20°C, creates a factor of power dissipation or watts.

All of this points out that the electrode count in an MLC capacitor has an enormous factor on the power dissipation capability of each design. Increasing the electrode count reduces the thermal resistivity which increases the power dissipation for a defined temperature rise. As such, with a given chip size, dielectric, and voltage rating, the capacitance dictates the number of electrodes, which in turn, dictates the power dissipation of the chip.

## Power Derating for Temperature

If the power dissipation capability of these devices is established with the industry quasi-standard of +20°C, then can that dissipation be constant up to the maximum temperature rating of the part? No, for if this were true, then a part in an ambient temperature equal to its maximum temperature rating will have an internal temperature that is 20°C above that rating. All established or monitored failure rates (or FIT) are verified at that maximum temperature, with a DC bias, and no AC currents. Dr. Reed [6] has shown that ripple currents offer no additional failure mechanism to a capacitor, other than creating an elevated temperature within the component above the ambient. It has also been shown that this elevated temperature creates the same reliability accelerations as if the part were tested at an ambient temperature equal to this elevated temperature, with no AC ripple.

As such, the power rating of a capacitor must be reduced as the ambient temperature approaches the maximum rating of the capacitor. Some early military specifications for leaded products allowed a +10°C rise at the maximum rating of the capacitor, but we believe that this could increase the failure rate by as much as a factor of three, over that established or monitored for this component.

In KEMET Spice, we reduce the allowable temperature rise at the maximum temperature to +2°C, or to a level within the measurement accuracy of the system. From this +2°C rise at the maximum, the rise increases to the defined allowed (+20°C is typical) at a temperature that is equal to the maximum temperature minus the rise. As an example, if the component is listed with an allowable temperature rise of +20°C, and a maximum temperature of 125°C, then at +125°C, the rise is reduced to +2°C, while at all temperatures below or equal to +105°C, the rise is the full +20°C (a linear interpolation is applied between +20°C at +105°C ambient, and

+2°C at +125°C ambient for any ambient temperature in between).

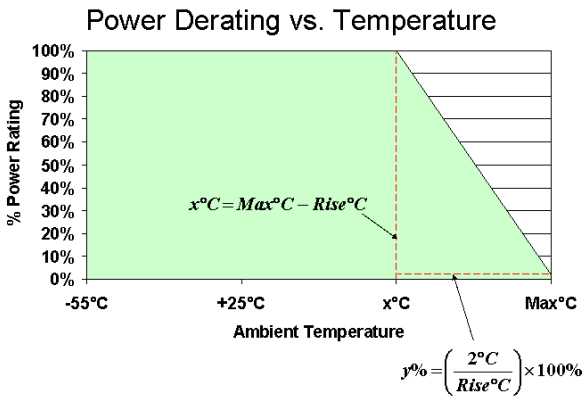


***Figure 11. Power derating for temperature***

Since we also allow the operator to change the allowable rise to any temperature up to +100°C, the allowable rise at maximum temperature is always restricted to +2°C, the ambient temperature at which the full rise is allowed is defined as the maximum temperature rating minus the rise (for a part with a maximum temperature of +125°C, and an allowable rise of +60°C, the point at which the power derating begins is at an ambient of +65°C).

## Future Revisions

This program has evolved over the past seven years and will continue to do so. We are constantly adding new part types as they are offered through the manufacturing process. Additionally, we are in the process of adding some of the new product offerings including stacked ceramic, high voltage, and high temperature families of capacitors.

We will also allow the operator to specify multiple capacitors to get the parallel effects. We will also include a combined impedance plot to see the cumulative response of multiple part types, and multiple pieces of each. Additionally, we will allow the operator to include scattering parameters as a choice for the ASCII file created of the frequency steps in the plot.

An automated notification process is available from our web site to notify you if there is a new revision available.

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