

Its success depends on the accuracy with which the individual components are depicted. The following article by John Prymak, a member of KEMET's Technology group, describes models of ceramic and tantalum capacitors we are developing to assist SPICE type circuit analysis.

John Piper, Vice-President Technology

SPICE Models of Capacitors

by John Prymak

SPICE is an acronym that stands for "Simulation Program for IC Emulation." This is a tool originally intended to aid in the understanding of the performance of integrated circuits (ICs). Today, SPICE modeling has moved beyond integrated circuit emulation to full circuit emulation. This tool is seen by many as an effective means of reducing cycle time from circuit design to manufacturing by eliminating most of the work needed in breadboard modification. However, its practical application is being hindered because components do not always behave as predicted. Unexpected parasitics and other effects unknown to the designer may result in a capacitance that is a tenth of what was expected, or even worse, the capacitor may be acting like an inductor.

The software available today for SPICE simulation are numerous and all different, with little compatibility. We started our analysis by using Mathcad® software to generate the frequency responses necessary, plus ASCII table listings of Frequency, Impedance, ESR (effective series resistance), Capacitance, DF, and Phase Angle throughout the chosen frequency spectrum.

The simple RLC model (Figure 1) is often considered fair representative of the component in varying frequency applications. Many papers and charts have depicted this model as representative of a capacitor's behavior over frequency. However, things are never as simple as they seem. For example, the resistive element changes with frequency, and electrolytic capacitors have a fairly steep capacitance roll-off at higher frequencies.

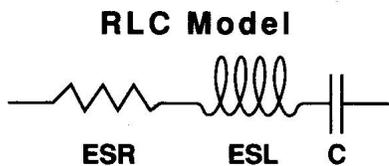


Figure 1

Ceramic Model

The ceramic capacitor model is distinguished by a frequency-dependent resistive element that seems to result in a minimum ESR at or near the self-resonance of the capacitor. The self-resonance is determined by the capacitance and ESL (effective series inductance) of the component. Because the capacitance change with the frequency is so little for the ceramic capacitor, it can be ignored. It can be shown that ESL is fixed by the design of the capacitor and as such, can be listed for each style and capacitance value. With the determination of self-resonance, the ESR can then be factored as the frequency moves away from the self-resonant frequency.

Impedance & ESR Bands based on Tolerance C0805C104K5

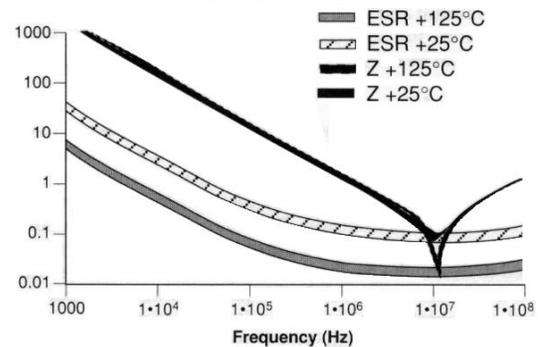


Figure 2

Figure 2 depicts the projected behavior of an X7R dielectric ceramic capacitor of 0.1 μF , with an ESL of 2.5 nH, over a frequency range from 1 kHz to 100 MHz. The band represents a range of typical performance with the capacitance tolerance ($\pm 10\%$) applied plus an additional $\pm 20\%$ tolerance to the ESR. No two pieces from a lot will behave exactly the same, but they should fall within this band of performance.

Figure 3 is representative of the model used in calculating the response throughout the frequency spectrum. The RLC components now show the ESR as temperature, frequency, and VDC dependent and the capacitance as temperature and VDC dependent. In addition to the series RLC components, there is an additional parallel resistance (the leakage resistance or insulation resistance) given as R_p , which is also temperature dependent. An additional RC network in parallel represents a capacitance that shunts the RLC elements, due mainly to that capacitance from the termination faces separated by the length of the chip. This is a very small capacitance and comes into play only at very high frequencies ($\geq 1\text{GHz}$).

Ceramic Capacitor Model

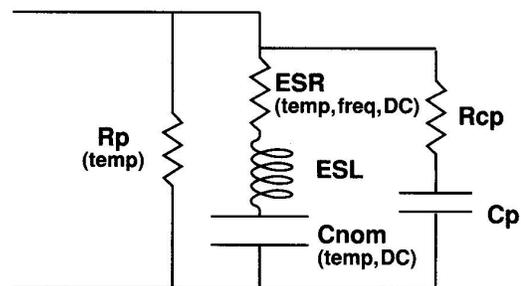


Figure 3

Additional dependencies applied to the ceramic model's elements include temperature and voltage effects. For X7R (Class II) and Z5U or Y5V (Class III) dielectrics, both capacitance and ESR will decay with applied DC bias. The rate at which capacitance for these devices decays is independent of their rated voltages, yet dependent on materials and designs. To establish conformity with the models, the voltage at which each capacitor loses 20% of its capacitance was arbitrarily selected as an additional point of information for calculating the ca-

capacitance drop due to DC bias. The relationship of decay is assumed as a first order approximation, to be linear through the -20% range. There is also a decay in ESR proportional to the capacitance drop with DC bias. There are no DC bias effects on capacitance or ESR for the NPO or COG (Class I) dielectrics.

The temperature affects both capacitance and ESR for the X7R, Z5U, and Y5V dielectrics, and affects only the ESR in any appreciable manner for the NPO or COG. For the NP0 at -55°C, the ESR will increase to approximately 2.4 times that observed at 25°C. At +125°C, the ESR will decay to 1/3 the observed ESR at 25°C. For the X7R, this relationship will be 3.6 times at -55°C and one-fifth (1/5) at +125°C. Both of these would appear as linear relationships on a semi-log plot (log ESR multiplier and linear temperature), and can be factored in the relationship. Figure 2 actually shows two bands of performance for the 0805 104 X7R: one at +25°C, the other at +125°C.

For Z5U and Y5V, the relationship of ESR versus temperature is similar to the X7R relationship up to +85°C. At this point, the ESR will reach its minimum and then start to increase dramatically. As long as the device does not exceed an application of +85°C, this unit's performance can be effectively predicted using the created models.

Tantalum Model

The tantalum capacitor brings the additional effect of frequency-dependent capacitance changes. Though the capacitance of a ceramic may decay by 1% per decade of frequency, this is insignificant in modeling the performance and is disregarded. The tantalum can decay 20% or more per decade. This has always been explained as a RC-Ladder type of phenomenon, and various RC-Ladders have been proposed to define the performance. There have even been instances where a model for a specific device has been detailed, yet none has included elemental definition (capacitance and resistance values for all values) for a series of capacitors. Figure 4 shows an RC-Ladder with consistent resistive elements between capacitive elements, and increasing capacitive elements as the depth increases in the ladder. This model was the simplest form to allow us to adequately fit the actual performance in terms of capacitance roll-off, impedance, and ESR with frequency.

This electrical presentation of the tantalum capacitor also fit with our understanding of the physical aspects of the capacitor: the capacitance decays with increasing frequency, and less of the signal penetrates the depth of the anode bulk. The capacitance available to the circuit at higher frequency is all located near the outer surface of the anode.

Again, the ESR is frequency sensitive, but tantalum capacitors appear to possess two nodes where the ESR changes slopes. The first lies between 1 kHz and 10 kHz, while the second appears near 10 MHz. The variance of the first frequency seems to be related to the size and materials of the anode, while the second appears to be independent and constant. Figure 5 shows a typical tantalum chip's behavior under different temperatures. Normally, the ESR and capacitance are allowed to vary according to their tolerances, but this band of performance was omitted here to reduce confusion.

With the tantalum capacitor, there is no noted effect of DC biases while the temperature affects only the ESR. This relationship is similar to the X7R ceramics, but at -55°C, the noted change is almost 3 times the 25°C ESR, and the +125°C ESR is one-fourth (1/4x) the

Tantalum Model

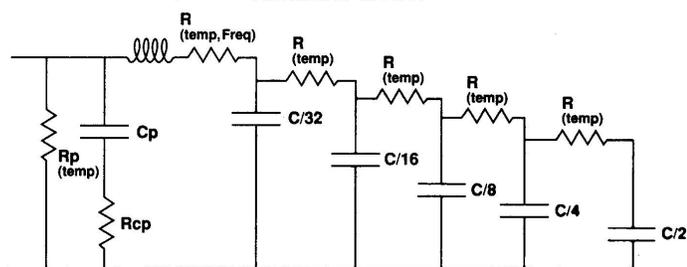


Figure 4

Impedance and ESR T491D476M010 @ -55°C, +25°C and +125°C

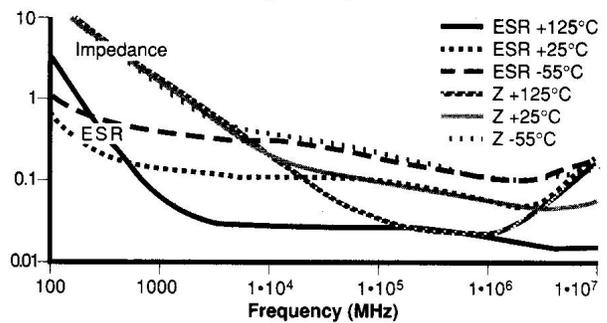


Figure 5
25°C ESR.

All the models generated were adjusted to allow them to duplicate typical responses from data gathered from the actual frequency scans of our components. Figure 6 depicts the projected typical response and that of an actual piece. This trace shows an almost perfect fit for this piece, but this piece represented a response very close to the average response for several pieces of this style. The allowance of the tolerance bands on capacitance and ESR accommodates the variations that will be seen from lot to lot and within a manufactured lot of pieces.

KEMET's SPICE Models

KEMET is striving to offer the best possible models to aid our customers in their SPICE use. Based on a survey conducted with our customers who use SPICE, we are using Mathcad® generated models with standard EIA values of 1206, 0805, and 0603 ceramic chips, of NP0, X7R, and Z5U (Y5V is coming). For tantalum chips we will offer a range of part types of different capacitance and voltage ratings for the T491 and T495 surface mount designs. The diskette offered contains the Mathcad® models (Version 4.0) plus an ASCII listing for each part type of frequency, impedance, ESR and capacitance at room ambient temperature and no DC bias. Additionally, for those who may be able to place the frequency, temperature, and bias relationships in their SPICE software, tables of sub-element values will be included for the ceramic and tantalum models for each specific capacitor type and capacitance.

Calculated and Actual ESR & Impedance T495X475M050

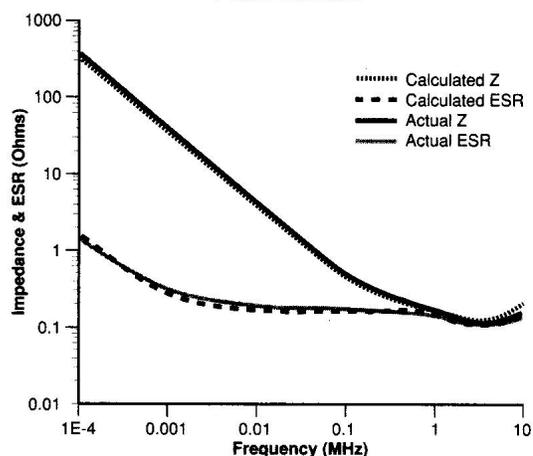


Figure 6

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