Capacitance Monitoring While Flex Testing

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F-2110 6/95

Reprinted 8/97

Flex Cracks

As most other modes of failure in surface mount multilayer ceramic capacitors have been dramatically reduced over the years, cracking due to stresses from boards bending has gained prominence.

The common printed circuit board (PCB) built of G10 or FR-4 glass epoxy materials will easily bend under moderate forces. Almost all processes involved in populating these boards can involve bending the board - many times unknowingly. High stresses transmitted to small areas of the board are of greatest concern. Manufacturing efficiencies improve by processing small PCBs as a group of multiple circuits within a singular "mother board." Depanelization, where the individual circuit boards are isolated from the "mother board," is one area where extremely high stress forces can be transmitted to the boards near the edges being cut. "Snap together" methods of assembly are also prone to creating these localized stress areas. The boards may be placed in a holder between process stages, where the outside edges are held and the board is allowed to droop in the middle. The board may be fitted into a cabinet or slot with a force that causes bending near an edge. Communication cables may be mechanically attached to an unsupported edge, translating all forces applied to the cable back to the board. These are just a few of the more common areas where board flexing can occur in assembly. These may be compounded if the board is later worked on in repair - especially by an impatient technician with a rubber hammer.

The bending of the board causes forces to be transmitted through the solder attach fillets to the surface mount chip. These forces are concentrated at the bottom of the chip, where the termination bands end. The mass of solder is important as this material is malleable, and slight amounts will move more freely. Forces applied very slowly will also allow the solder to stretch and absorb some of the force. Excessive solder leads to a greater susceptibility to thermal shock.Also keep in mind that all the thermal shock studies support a moderate amount of solder.

The ceramic material is hard, non-elastic, and brittle. The shear force pulling at the ceramic along the termination edge will lead to a crack if the forces are sufficient. At what force the chip cracks is thought to be dependent upon the ceramic material, the amount of solder, the termination materials and amounts, and possible defects or anomalies within the ceramic structure.

Figure 1 details a typical flex crack at one of the termination ends. Remember that this is a two-dimensional representation of a three-dimensional phenomenon. The crack always starts near the edge of the termination margin, then extends upward toward the termination face. The angle that this crack takes is usually around 45°. The crack may extend into the termination face, thereby separating a corner section. It may also turn upward toward the top face of the chip, where it will usually turn out towards the top termination margin's edge. This crack may cause the entire end of the chip to be separated from the main body of the chip.

The angle may change with different dielectric types and applied forces. The crack's exit usually takes place beneath the termination margin and is not apparent on visual inspection. As the force is applied, the crack

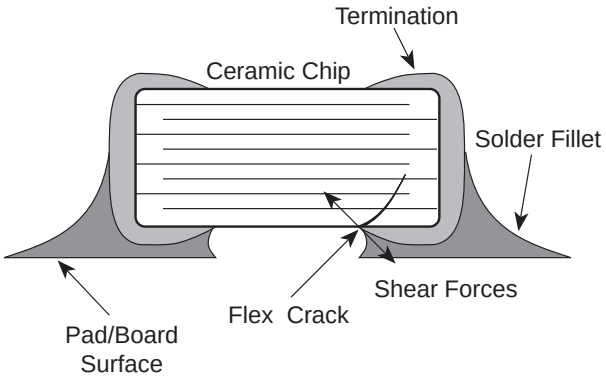


Figure 1. Flex Crack - Cutaway View

causes separation along its path, and disconnection of one or more of the electrode plates. Be aware that as this force is removed, the separation may be eliminated and allow the disconnected electrode to return and connect again. Because of this return, it is possible to test a "cracked" chip for capacitance, dissipation factor, and insulation resistance, after removal of the flex forces, and read the cracked unit as a good capacitor with no apparent fault.

Flex Testing

This testing, called "flex," "bend," or "warp" testing, was instituted to detect a susceptibility to these forces. There are different methods in the industry for applying the bend stress, but the board layout is consistent. As shown in Figure 2, the board dimensions are 100mm x 40mm x 1.6mm and of the G10 or FR-4 type that is detailed in *EIA-J RC 3402*. The chip is to be mounted at the center of the board, with its opposite termination pads straddling the center line of the board. As with all surface mount applications, the amount of solder and

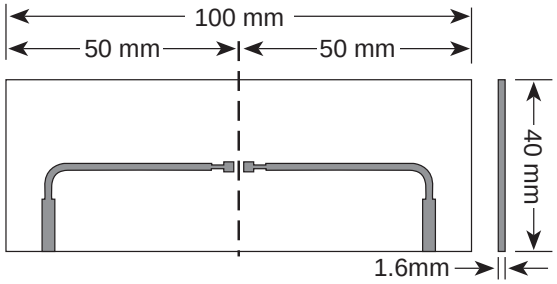


Figure 2. Board Dimensions

the dimensions and separation of the pads are crucial to obtaining a good mounting of the chip. These pad dimensions vary with chip size but always maintain the chip at the center of the board.

The apparatus for flexing the chip consists of a ram along the centerline of the board, pressing into the board at a constant rate. The board is held along its edges, at a spacing of 90 mm as seen in Figure 3. The application of the ram into the board is to be at a constant rate of 20mm per minute.

We use a stationary ram and moved the block holding the board down into the ram as in Figure 4. The

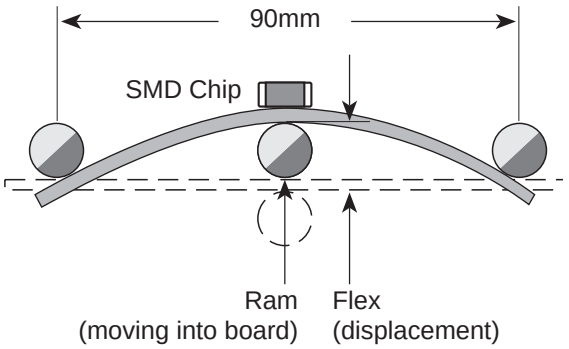


Figure 3. Flex Test Mechanism

movement of the ram into the board is generated by a motor attached to a screw drive, controlling the movement of the block. The motor is a constant speed DC motor which allows us to control the direction of the block movement. By selecting the right gears, we are able to achieve a speed of 20mm per minute.

The specification *EIA-J RC 3402* details the ram as having a radius of 340mm with a 20mm width. The length of the ram is greater than the width of the board,

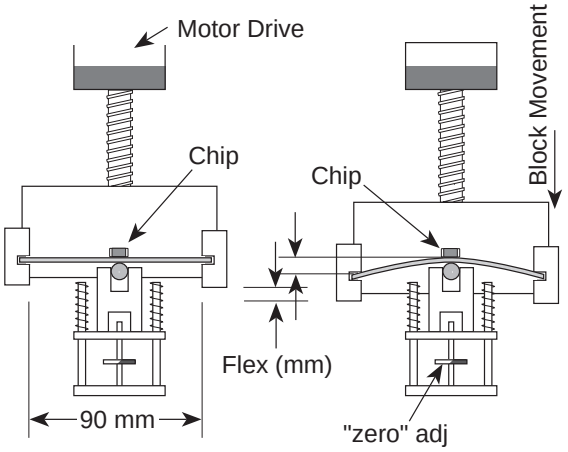


Figure 4. Tester

allowing it to extend beyond both edges of the board while presenting the force all along the center line. In the EIA-J specification, this ram was initially specified for applying board deflections of 1mm as a "proof test." Higher deflection is required, especially for manufacturers like us where 1mm was not generating any failures. We need to consistently generate > 50% failures to get an understanding of the physics of the failures and to allow comparisons.

A ram radius of 340mm also restricts the maximum curvature that can be applied to the board. If a board were to bend uniformly between the 90mm edges, then at 3mm, the radius of the ram would form a perfect fit for the curved surface of the board. Bending beyond this would cause a concentration of the increasing curvature along the outside edges of the ram at 20mm separation (Figure 5). There would be decreasing radius of the board beneath the chip, but this would be indeterminate and unrelated to the travel of the ram.

A proposed EIA specification, *EIA Proposed Draft PN-2271*, defines the radius of the ram as 140 mm. If the board was to bend uniformly between the 90mm edges, this ram would form a perfect fit to the surface of the board at 7.5mm deflection. Papers have been presented where this ram was used in testing up to 12mm of deflection. The data generated from travel beyond 7.5mm now becomes suspect.

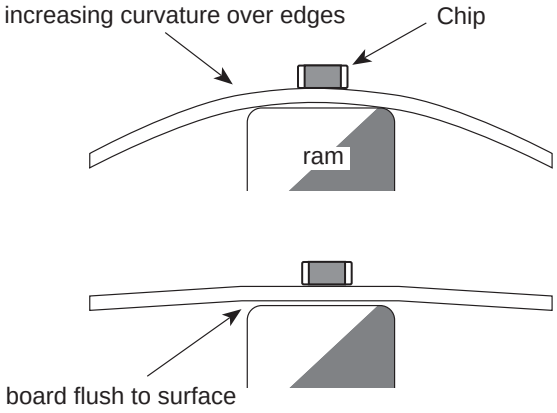


Figure 5. Curvature of Board to Surface of Ram

The board does not bend uniformly (Figure 6). It will tend to curve more along the edge of the applied force, with decreasing curvature as the distance from its application point increases. Its shape is more parabolic than that of a uniform arc. To avoid these effects and particularly to avoid changes in the manner in which stress is applied as the deflection increases, we chose the narrow ram radius of 5mm. The increasing curvature of the board will be at an accelerated rate over that based on the assumptions of an ideally curved board, but the comparisons are all with the same equipment, material, and conditions. In fact, because of this parabolic effect exhibited by the board, the 340mm radius ram will actually fit the board *before 3mm*, and the 140mm ram will also fit *before 7.5mm*.

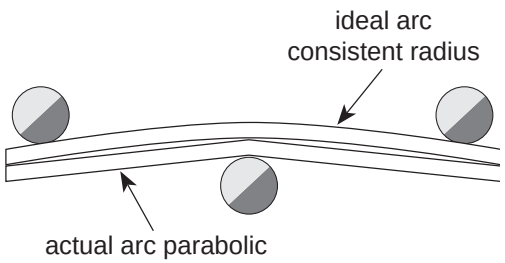


Figure 6. Ideal Arc versus Actual

Test Criteria

After defining equipment and materials, the procedure for testing and criterion needs to be established. Here is where most of the variations occur with this test. The requirement listed in the *JIS-C- 6429* document details that the board be flexed to 1mm, held there for 5 seconds, capacitance measured, then returned to a

"no flex" state. Capacitance is compared to the initial value to determine if a crack has occurred. With consideration that the X7R, Z5U, and Y5V dielectrics have a high piezoelectric characteristic, they allow the capacitance to change 12% for these devices before it is declared to have failed. For NP0 dielectrics, the allowable change is 5% or 0.5 pF, whichever is greater. Consider that with any capacitor built with more than nine effective layers, loss of one layer will cause a capacitance loss of less than 12%.

One variation of this test is to bend the board a number of cycles and then measure for a capacitance shift. Another variation requires the chips to be placed in a humidity chamber at elevated temperatures and relative humidity, then measured for insulation resistance 24 hours later. Still another variation calls for flex exposure in increasing magnitudes of 0.5 mm, with capacitance checks in between each progressive bend.

The criteria for all of these methods result in a "go and no-go" declaration. Multiple groups subjected to this testing could result in being "all good" or being "all bad." There was no way of distinguishing among the "all good" batches or among the "all bad" batches. Manufacturing changes involving design, process or material changes were lost many times within these common declarations where there appeared to be no difference among the groups. A more exacting indication was needed to determine exactly when each unit failed.

Monitoring Capacitance

The specification *JIS-C-6429* outlines procedures where the capacitance is tested while the board is under flex. The board is built with traces extending to the edges to allow capacitance or insulation resistance testing of the chips before and after flex exposure. These traces can be used to continuously monitor the unit while it undergoes the flex test. Combining a computer and capacitance meter to monitor the capacitance with time allows an instantaneous translation of time to distance. A comparison of capacitance with flexure is now available. Utilizing an optically isolated relay board controlled by the computer, the entire test apparatus was automated to allow the computer to control the initiation and then monitor the capacitance versus flex.

A typical response is shown in Figure 7. At 5.6 seconds into the test, the deflection is ~ 2.1mm and the capacitance drops suddenly. Prior to this there is some wavering of the capacitance. In many cases, steady decay in capacitance of nearly -15% will precede the sudden drop. What is most interesting in this response is that the capacitance eventually returns to 99 nFd, as if there were no change at all. The change is only +1% based on the initial reading of 98 nFd. Initial and post-capacitance measurements would have declared this capacitor as being "without crack." The initial and post-dissipation factor also gave no clue, as it returned to 2.38% from an initial value of 2.42%.

Our test criteria became any sudden capacitance change between consecutive readings greater than 2% for the higher dielectrics, and 1% for NP0 dielectrics. The return to initial capacitance occurred in about 30% of the pieces tested. Some lots had greater incidence of this while some had no units return to the original reading. We attempted to stop many units when the

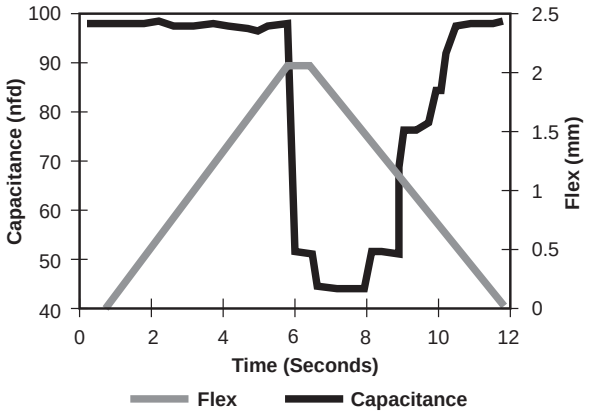


Figure 7. Capacitance Drop ~2mm

sudden change may have been 3% to 10%, but because of the lag time with the capacitance meter reading and transmitting the reading to the computer, the capacitance usually decayed additionally to near 0. Considering the elastic nature of the crack propagation, this small capacitance change may have been a momentary change on its way to the larger change, regardless of the response time.

In large quantity tests, the unit is electrically disconnected as soon as the computer signals a crack and starts to return to 0mm. The next board is electrically connected and swapped into the fixture as soon as the flexure returns to 0mm. The operator starts the next board as soon as the computer signals that it is acceptable to do so. A 50-piece sample can be read in under 30 minutes.

Analysis of the Data

The data was not analyzed while the test was taking place but stored for later analysis. The analysis included ordering, cumulative failure distributions and linear regression to allow projection of the flex needed to achieve a chosen extrapolated failure rate of 100PPM. The variance (R^2) had to be greater than 95%, and typically, values of 98% were achieved. If the R^2 was less than 95%, then the data distribution pattern was reviewed to see if multiple linear regressions would better fit the data. Figure 8 shows the data and the two linear regression fits. Almost all the groups show some sort of bimodal distribution. We have analyzed many groups in an attempt to explain this effect, but we have not been successful to date. In all cases, the slopes decay as the average flexure of each of the bimodal groups within the total distribution increases.

The number of pieces in a sample tested initially was 25, but we soon progressed to 50 pieces to obtain more confidence in the analysis. Sample groups of 100 give even greater credence to the results and are preferred when comparing process or material variations that might lead to minor differences. The data analysis, from input through the first fit, is automated as a macro in the spreadsheet software used. Additional analysis is dependent upon user's input as to what data elements are to be used for each regression.

The end user of these chips is more likely to be concerned about the minimum flex levels than at what flex level 50% failure is achieved. There are many

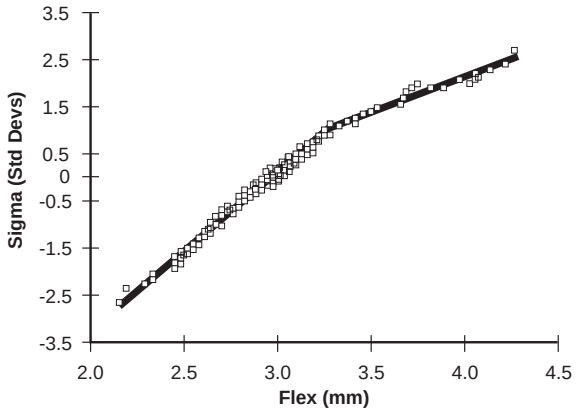


Figure 8. Cumulative Dist. - Standard Deviations

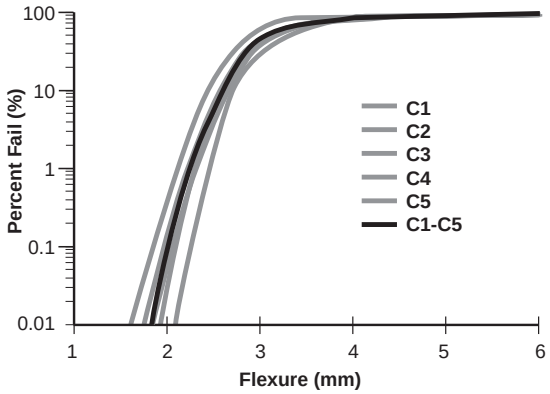


Figure 9. Same Lot Tested in Five Different Samples

cases where the 50% failure levels contradict the 100PPM rates. For these reasons, comparison of lots should be based on the 100PPM failure levels. For groups with multiple regressions, we use the 100PPM level indicated by the lower flex group as the comparative number.

To establish a consistent test, sample preparation and procedures are important aspects that must be controlled as tightly as possible. The application of the solder to the pads is critical. On the basis of chip size, we use an air-driven dispenser with preset air pressure, nozzle size, and duration for the solder paste application.

To establish the consistency achieved, a sample was divided into five distinct batches. The first three, C1 through C3, were mounted to the test boards, all on the same day. The fourth lot, C4, was mounted a week later, and the last lot, C5, was mounted a week after C4. Two of the first three lots, C1 and C2, were flex tested 24 hours after mounting. Lots C3 and C4 were flex tested 24 hours after C4 was mounted. C5 was tested 24 hours after it was mounted, one week after C3 and C4. Additionally, all the data from Lots C1 through C5 was combined to analyze the overall data compared to the individual groups. C1 through C3 were to give us an idea of consistency for the test process and the additional groups of C4 and C5 were to give us an indication of our mounting consistency.

The results of the consistency test achieved are depicted in Figure 9. Table 1 (page 6) lists some of the more important aspects of each of the groups, including 100PPM failure flex (mm), average failure (mm), and the flex (mm) needed to achieve 0.1%, 1%, 5% ,and 10% failure rates.

Variations in Manufacturing

Once we established our consistency in testing , we looked at the consistency that was achieved with a given product manufactured over a period of time. From production batches spanning a 25 week period, we gathered 11 groups of 1206 and 8 groups of 0805, X7R, 104 chips. Figure 10 depicts the range in the calculated linearizations for these groups and Table 2 lists the same parameters as used in Table 1, for the best and the worst of these 11 groups. This variation is not much greater than our consistency spread and leads us to believe that our materials and process result in a fairly consistent product.

Effects of Chip Size on Flex Strength

The movement of the industry is towards smaller chip sizes. The 1206 chip is being replaced by the 0805, 0603, and 0402 sizes. Data from five groups of 0805, X7R, 104 chips were combined to show the difference between these groups and the 1206 data previously established. The 1206 data is the same C1-C5 data discussed earlier. These chips are of the same material and capacitance, with the design changed in the smaller

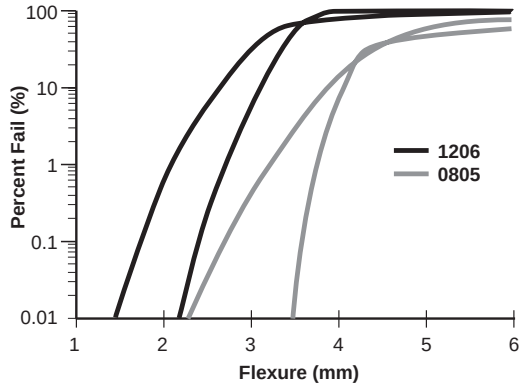


Figure 10. Manufacturing Variations

chip to a thinner dielectric thickness.

It is readily apparent in Figure 11 that the smaller chip has a greater flex capability. The thinner dielectric is not the cause of the increased flex capabilities, as parallel experiments showed this to be of indiscernible effect. To understand why the increase in flex capability exists, consider that the distance between the terminations has decreased with the 0805 from the 1206. The flexure force, as an increasing curvature between two fixed points, generates a stress force that is proportional to the increasing arc distance between these points. The growth can be seen as fractional, and with the larger separation of the 1206 chip, the growth in the length of the arc is greater than with the 0805.

If the forces were truly proportional to the distance between the separations, then we should be able to establish this effect with a known group, terminated with varying margins. We created two additional test batches from the same production lot of chips used for the C1-

Table 1. Repetitive Testing - 1206 X7R 104 50V

Sample	100PPM @	Avg @	0.1% Flex	1.0% Flex	5.0% Flex	10% Flex
C1	1.83	2.97	2.02	2.26	2.47	2.58
C2	1.84	2.89	2.01	2.23	2.42	2.52
C3	1.75	3.03	1.97	2.23	2.46	2.59
C4	1.98	3.03	2.15	2.37	2.56	2.66
C5	1.64	2.81	1.83	2.08	2.29	2.40
C1-C5	1.84	2.95	2.02	2.25	2.45	2.56

Table 2. Manufacturing Variations-1206 X7R 104 50V

Lot	100PPM @	Avg @	0.1% Flex	1.0% Flex	5.0% Flex	10% Flex
1206 Best	2.21	3.43	2.41	2.67	2.89	3.01
1206 Worst	1.41	3.33	1.73	2.13	2.48	2.67
0805 Best	3.50	4.33	3.64	3.81	3.96	4.04
0805 Worst	2.29	4.55	2.67	3.14	3.55	3.77

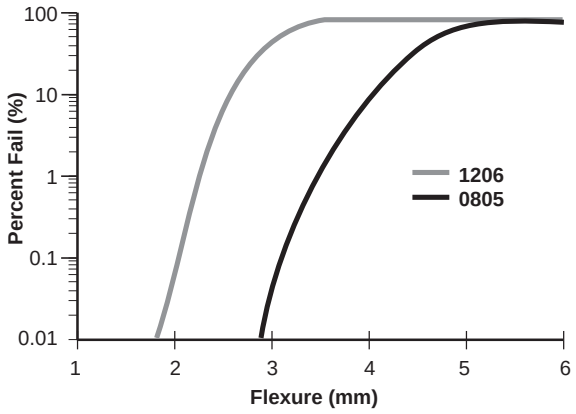


Figure 11. 0.10 μFd, X7R 1206 versus 0805 Chip

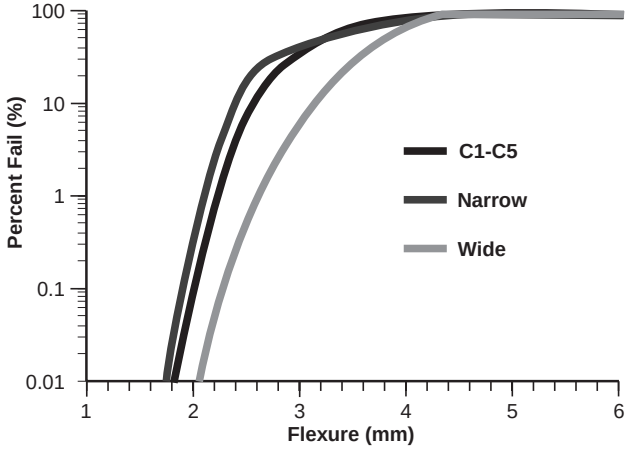


Figure 12. Effects of Margins on Flex Testing

C5 experiments. With one group, we attempted to create smaller margin overlaps, or bands by dipping the chip ends in the silver paste termination material to a depth ~ 15 mil less than standard (25 mil). Large overlaps or bands were created by dipping the chips in the silver paste to a depth ~ 15 mil deeper than standard. The cumulative change in separation for these narrow and wide band chips was ~ 30 mil between them, or ~ - 15 mil for the narrow band and ~ + 15 mil for the wide bands over the standard production bands. Figure 12 shows the results plotted for this study. From left to right, the three curves represent the narrow termination bands, the normal bands, and the wide termination bands. The data supports the hypothesis that the wide silver bands with narrow gaps between them, have the highest flex strength.

Competitive Analysis

We tested eight different groups of 1206, X7R, 104 chips from five different vendors, and six groups of 0805, X7R, 104 chips from five different vendors. The range of best to worst for each of the chip sizes is shown in Figure 13. These wide ranges of response deal with raw material formulations and process conditions that may vary considerably from our own and among these manufacturers. The crossing response in the 0805 chip ranges highlights that there are very significant dissimilarities. This comparison allows us to judge the effectiveness of our product compared to others for flex strength considerations.

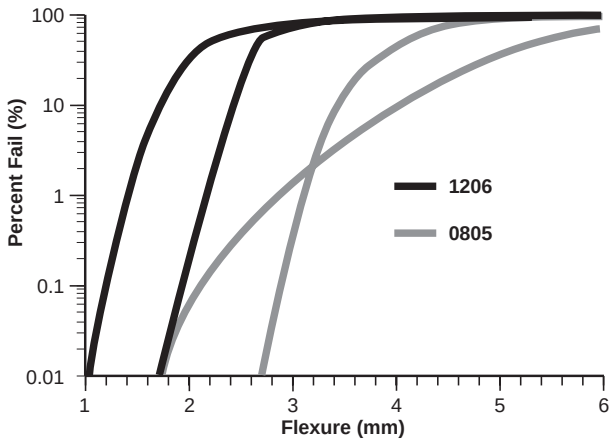


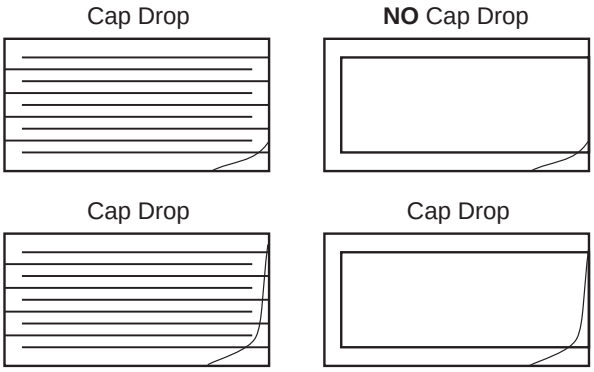
Figure 13. Competitive Product Range

Electrode Plane Considerations

In the analysis of the 0805 chips, we found some of the groups whose chips had thickness very close to their widths. With all the testing to this point, the chips had thicknesses that were considerably less than their width. As such, when mounted in their lowest profile, the electrode planes were always oriented to be parallel to the plane of the board. With those chips whose width and thickness were not distinct, there was no way of knowing what the electrode plane orientation was. Mounting was usually a 50/50 distribution of chips with electrode planes parallel to the board and those with electrode planes perpendicular. This variation did show significance in some of the tested lots. In the bimodal

distributions, it was noted that a large percentage of those pieces with very high flex strength had their electrodes perpendicular to the plane of the board. This alone did not define the bimodal effect, as there were many units with electrode places perpendicular to the board distributed among the lower flex failures.

This effect does point out a deficiency in this test. Looking at Figure 14, and remembering that this is a two-dimensional representation of a three-dimensional effect, the unit in the upper right corner would show no loss of capacitance in this test. If the corner of the electrodes in the adjacent planes were severed by this crack, the loss in capacitance would probably be less than 2%. (Remember that the crack would extend into and out of the two-dimensional cutaway view, and the electrodes in the adjacent planes are connected to the opposite termination end.) The crack would have to extend upward into the chip, high enough to sever the



Three of these four would register as cracked when monitoring capacitance. The cracked unit shown at the top right would read no change in capacitance.

Figure 14. Parallel and Perpendicular to Board Plane

electrode completely as in the lower right chip. The undetected crack that traverses electrodes offers the same insidious potential of failure as any crack detected, irrespective of the capability of detection in this test.

Reverse Flex

Chips have also been tested with the board reversed, so that the chip is on the concave side of the flexed board (Figure 15). A slot in the ram allows spacing between the ram and the chip, preventing physical contact between the two. In this test, the ram was driven to a flexure of 10mm, held for 2.5 seconds, then gradually withdrawn as the data of Figure 16 represents. We also ran this test with an increase in the hold to 10 seconds as indicated in Figure 17. In every case, the chip failed during the *withdrawal* of the ram and relaxation of flexure. With a 2.5 second dwell at the maximum flexure (Figure 16), the failure occurred at 6mm into the withdrawal. With the longer dwell the failure occurred sooner, at 4mm into the withdrawal. Averages for 10 pieces tested in each condition were:

Condition	Distance to Failure
Reverse Flex (10mm), 2.5 sec. dwell	5.2mm from peak
Reverse Flex (10mm), 10 sec. dwell	4.7mm from peak
Normal Flex (10mm maximum)	4.4mm from start

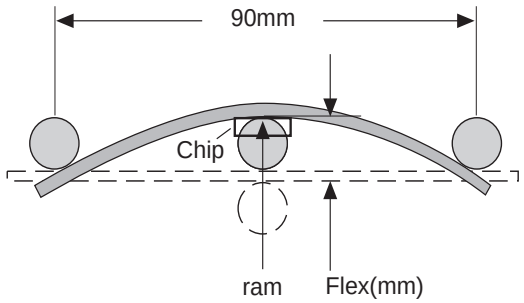


Figure 15. Flex Test with Chip on Bottom Side Reverse Flex

Solder is a malleable metal. During the application of reverse flex, the chip is predominantly under compression (Figure 18). The compressive strength of ceramics is usually high, so the force will not damage the chip unless it has a substantial fault such as a delamination. The solder fillets, however, gradually deform outwardly to relieve the stress applied to them. When the board

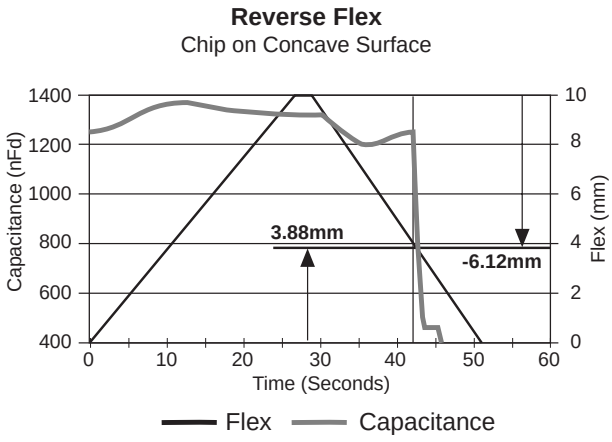


Figure 16. Reverse Flex with 2.5 Second Dwell

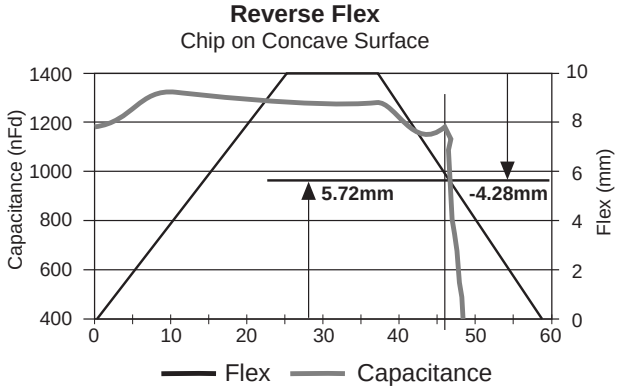


Figure 17. Reverse Flex with 10 Second Dwell

flexure is reduced, the partially deformed fillets cause the chip to experience increasing tensile stresses, and failure occurs in a similar manner and with a similar characteristic crack to that observed with normal flex testing. The longer the dwell at maximum flexure, the more stress-relieving deformation of the solder; hence,

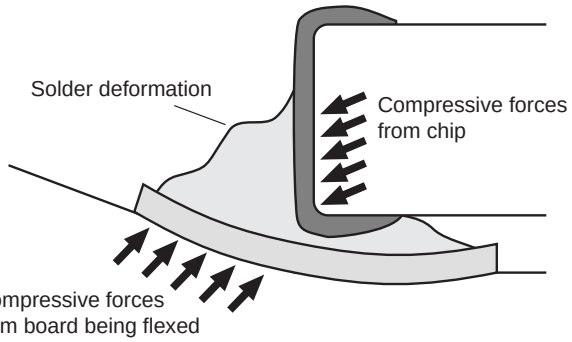


Figure 18. Solder Deformation on Reverse Flex

the earlier tensile builds on the chip during withdrawal of the ram.

It is unlikely that reverse flex testing will add chip-related information beyond that obtained with normal flex testing. However, the reverse flex test does illustrate the impact of solder properties on the flex test, and the need to conduct the test so as to minimize solder-related variation by considering:

a) amount of solder in the fillet,
b) composition/mechanical properties of the solder,
c) rates of increase or decrease of stress on the solder joints.

It is now evident that the forces causing the crack in both the forward and reverse flex are the same – with the resulting cracks also the same. As such, visual examination cannot be used to determine in which direction the flexure was applied to cause a crack.

Acoustic Emission Monitoring

Another method proposed for crack detection deals with acoustic emission detection. The crack will generate a high- frequency, low-level acoustic scream as it jumps through the dielectric. With the use of a transducer and the appropriate amplifying equipment, these acoustic sounds can be readily detected. This can detect cracks if they do not traverse electrodes and regardless of electrode orientation, but may also capture false triggers as crack initiations.

As the board is held at the separation of 90 mm during the bending, its arc length is a greater distance between these points. The distance at 0 mm flex is 90 mm, but at 10 mm flex, the arc distance is now 92.9 mm between these two fixed points. During the transition from 0 to 10 mm flex, the board will slide along the edges to allow for this greater length requirement. This slide is not a continuous one but jumpy, occurring intermittently through the transition. These jumps will translate a sudden stress change to the capacitor under test. If the dielectric has a potential for piezoelectric noise, the resulting ring within the ceramic could be interpreted as an acoustic signature from a crack.

There is also the possibility that a benign crack would cause determination of failure. Such a crack could start as all flex cracks but jump immediately to the termination face without traversing any electrodes (Figure 19). This crack would never in itself lead to a failure, but the acoustic emission test would regard it to be an equal

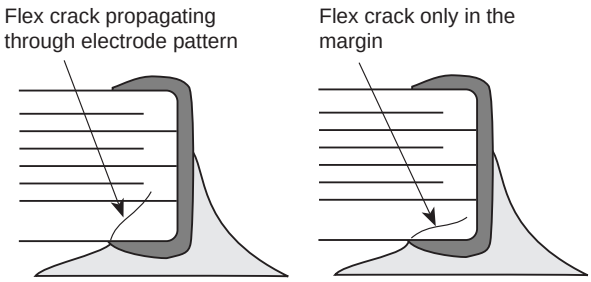


Figure 19. Both Cracks Detected by Acoustic Emission

failure to the unit where the entire termination end is severed from the main body of the chip.

Conclusion

This testing establishes a tool to allow us to continue our efforts to continually offer the best product available. It is readily available to manufacturers and users alike. With the considerations presented, the results are very repeatable and the test is consistent.

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