

The Battle for Maximum Volumetric Efficiency – Part 2: Advancements in Solid Electrolyte Capacitors

**Michael Randall, Tony Kinard, Javid Qazi,
Randy Hahn, Philip Lessner**

KEMET Electronics Corporation,
P.O. Box 5928, Greenville, SC 29606

Phone: 864-409-5611, FAX: 864-409-5642
e-mail: mikerandall@kemet.com

**Susan Troler-McKinstry, Song Won Ko, Sheng-guo Lu,
Tanawadee Dechakupt, Clive A. Randall, Elizabeth Dickey**

Pennsylvania State University, Materials Research Laboratory, State College, PA 16801

Abstract

Increasing need for capacitors with higher capacitance per unit volume has led to development efforts resulting in impressive combinations of dielectric thickness, dielectric constant and active area per unit volume. In order to achieve these developments, traditional Ta capacitor and multilayer ceramic capacitor (MLCC) technologies have evolved to surprisingly high levels of sophistication. These efforts have resulted in substantial increases in capacitance volumetric efficiency (VE_C) over time; rates that rival or exceed the rate of Moore's law for integrated circuit (IC) advancement.¹ In order to continue along this path, both valve conductor (e.g. Ta) and MLCC technologies face major challenges. This paper discusses these challenges from both materials and packaging developments perspectives. High VE_C -enabling technologies for traditional solid electrolyte capacitors are discussed, as well as a new, high dielectric constant (ϵ'), hybrid dielectric technology for electrolytic capacitor systems. Both development approaches have the potential to increase VE_C several-fold for future capacitor devices and have the potential to be used in combination to achieve even greater increases in VE_C .

Introduction

Arguably the greatest driver for advancement of capacitors developed for surface mount electronic applications is volumetric efficiency (VE_C). Over about the past decade multilayer ceramic capacitor (MLCC) technology has become increasingly competitive with solid electrolyte capacitor (SEC) technology from a VE_C standpoint as indicated in figure 1. The rate of advancement of VE_C for MLCC has been approximately double that of solid electrolyte capacitors. Other advantages of MLCC over SEC are that capacitance rolls off more slowly with frequency as indicated in figure 2. Additionally, MLCC typically exhibit reduced equivalent series resistance (ESR) as illustrated in figure 3.² MLCC also have detractors when compared to SEC. Class 2 and 3 MLCC exhibit significant capacitance loss due to dielectric aging, capacitance temperature sensitivity and capacitance electric field sensitivity that can reduce VE_C as much as 60% or more as indicated in figure 4 for a typical X5R (Class 2) dielectric system. Under these situations, the analogous Ta SEC capacitor will exhibit largely stable VE_C properties over the same range of temperature and operating voltage/field. Thus, the designer needs to select between the relative stability of SEC with respect to time, temperature and electrical field vs. the relative frequency stability and low ESR of MLCC.

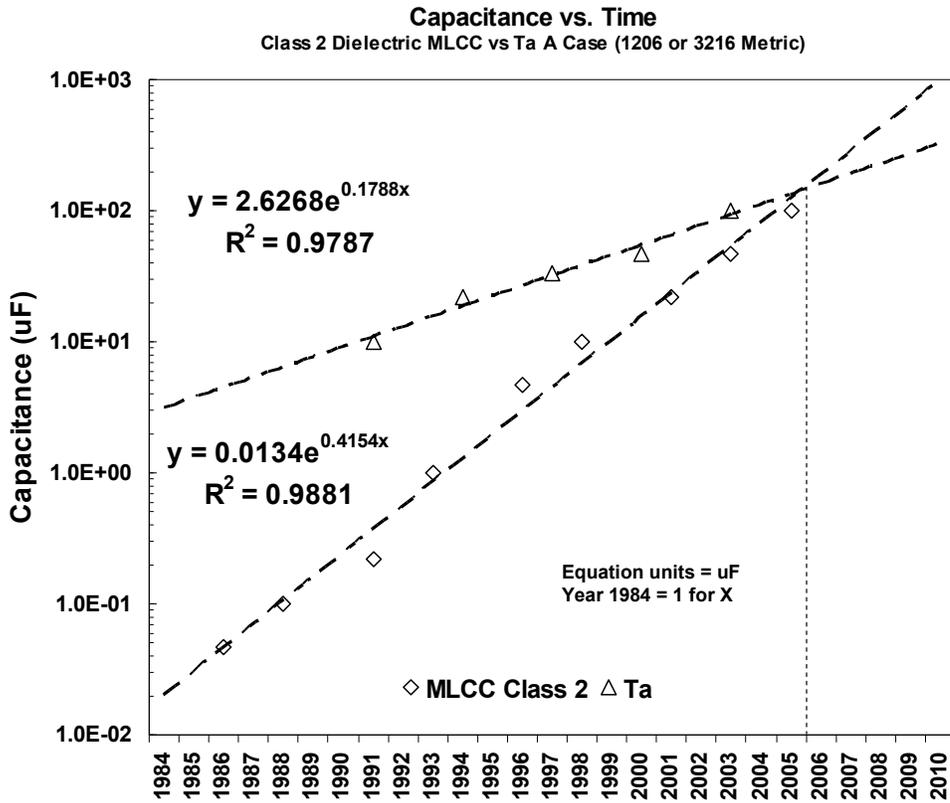


Figure 1. V_{EC} vs time for Ta solid electrolyte capacitors compared with MLCC

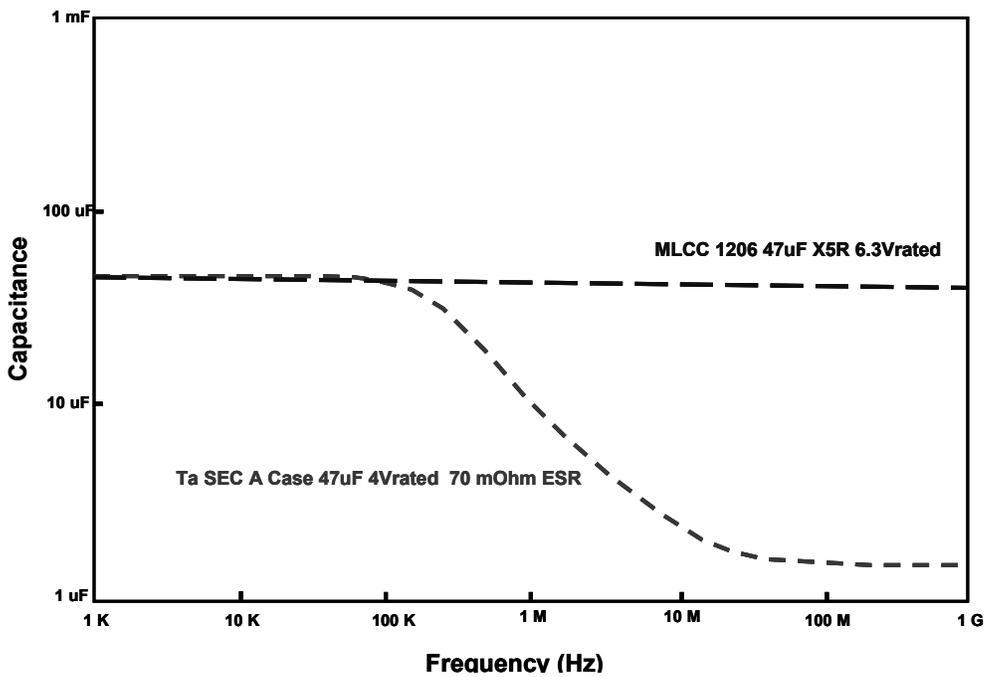


Figure 2. Capacitance vs. frequency for Ta polymer SEC compared with analogous MLCC

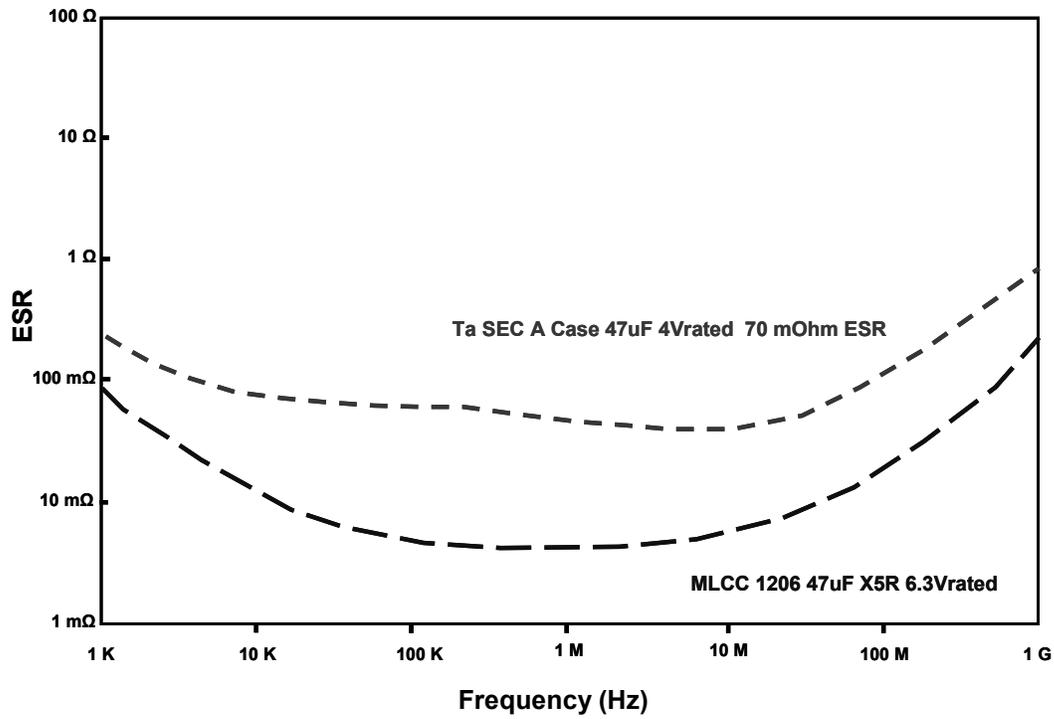


Figure 3. ESR vs. frequency for Ta polymer SEC and analogous MLCC

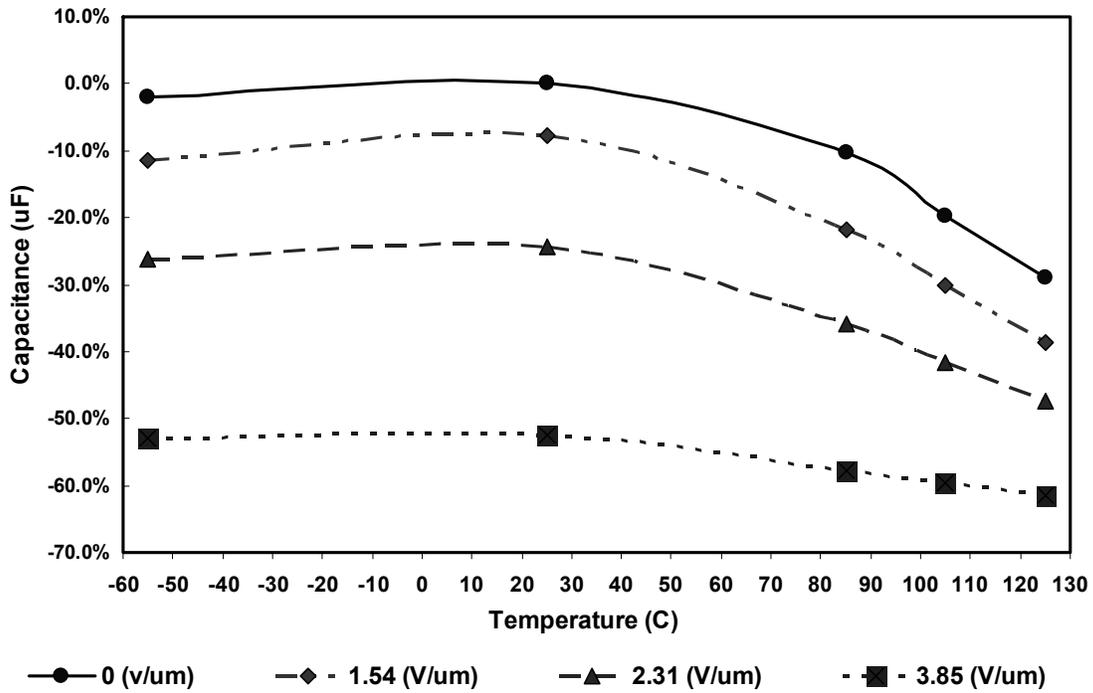


Figure 4. Capacitance vs. Temperature and Voltage for a typical high V_{EC} X5R dielectric MLCC

Other factors are important considerations for the selection process as well, but the primary selection criterion for most applications is typically VE_C , the subject of this paper.

In the “ VE_C war” between MLCC and SEC the rate of progress of VE_C or capacitance growth rate within a given package size has been quite significant as illustrated in figure 5. The growth rate for MLCC has been significantly higher than for SEC. However, it is likely to slow over the next few years as dielectric thickness (t) is pushed ever thinner. The result of this reduction in t is due to the commensurate reduction in grain size of the ferroelectric X5R materials in order to fit a required number of dielectric grains within the decreasing thickness of the dielectric layers with time. This will likely result in a reduction in the dielectric constant (ϵ') of the barium titanate (BT), which is used as the basis for most X5R dielectrics.^{3,4} Projecting a logarithmic relationship for ϵ' for X5R vs. grain size^{3,5} it is possible to predict a new rate, modified for this effect, assuming that all other rates of advancement (i.e., reduction in dielectric thickness, electrode thickness and inactive volume, etc.) continue as projected to meet the rate illustrated for MLCC in figure 1. The modified curve is illustrated in figure 5. Additionally, the rate of increase of capacitance per unit volume for SEC will likely increase due to efforts to reduce inactive volume by raising the packaging efficiency (PE_C), as well as to improve VE_C of the active volume as discussed in this paper.

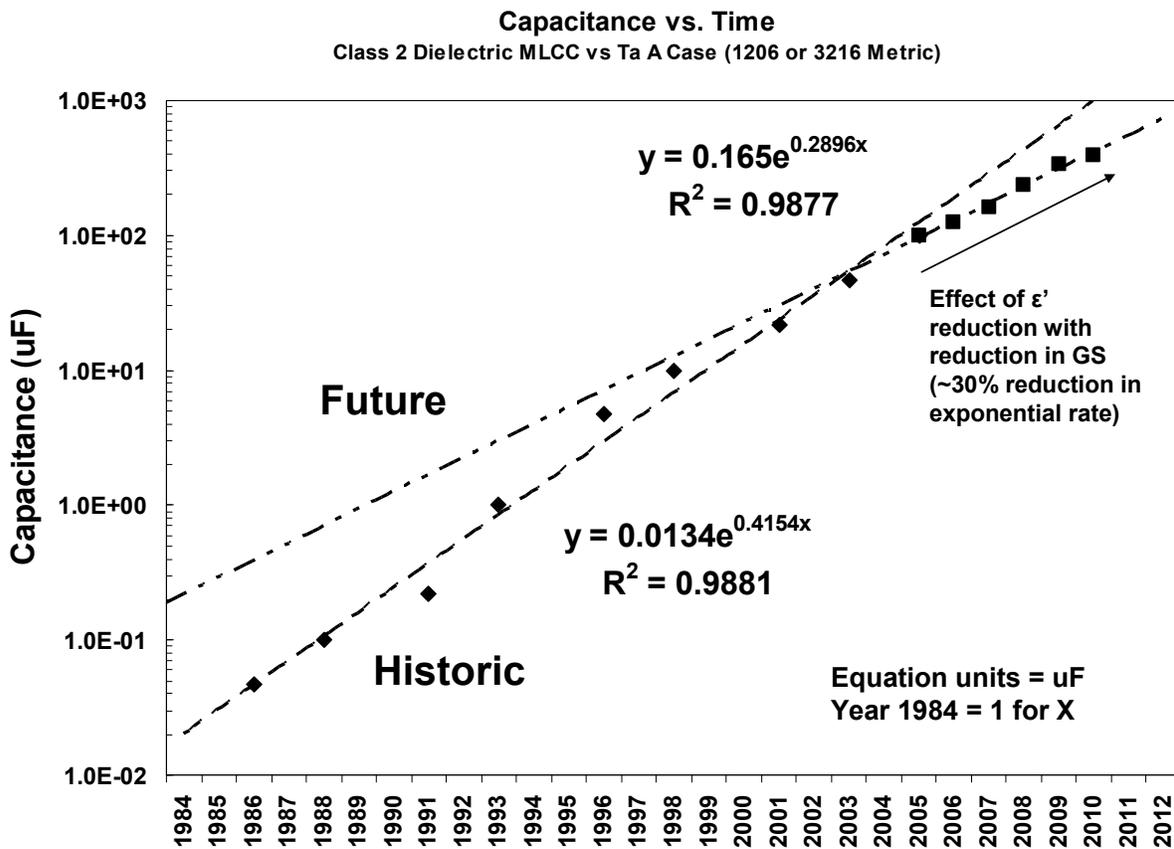


Figure 5. Projection of capacitance vs. time for MLCC considering a reduction in ϵ' as grain size is reduced to accommodate thinner dielectric layers

The generic equation for capacitance of a single dielectric layer sandwiched between 2 electrodes is

$$C = \frac{\epsilon_0 \epsilon' A}{t}$$

where:

C = Capacitance (Farads)

ϵ_0 = the dielectric permittivity of free space (8.854×10^{-12} F/m)

ϵ' = the dielectric constant of the dielectric within the capacitor

A = overlap area (m^2)

t = dielectric thickness (m)

From this equation, it is evident that the capacitor system characterized by the highest ϵ' and A and the lowest t per unit volume will have the highest VE_C . Depending upon the capacitor type, however, capacitor developers go about maximizing this combination in different ways. In the case of MLCC, high VE_C is achieved via high dielectric constant (ϵ') combined with a relatively high percentage of active volume per unit volume, but with relatively thick dielectric (t) compared to SEC systems. MLCC development efforts to achieve maximized VE_C typically focus on reduction of t as the VE_C of MLCC is increased as the square of t is decreased following the relation

$$VE_C \propto \frac{1}{t^2}$$

Traditional MLCC are made using a “thick film tape” process that results in relatively high values for t_{MLCC} compared to t_{SEC} . The dielectric in SEC is typically fabricated using an anodization or formation process that results in low values of t_{SEC} relative to t_{MLCC} (e.g., ~50 nm or less for SEC vs. ~800 nm for MLCC). This is possible, in part due to the relatively high dielectric breakdown strengths of valve metal dielectrics (e.g., Ta_2O_5) compared to those of MLCC dielectrics (BaTiO₃-based), but also to the fact that the dielectric fabrication process for SEC is largely “self-healing” (i.e., the anodization process inherently tends to form oxides in regions of relatively high conductivity, reducing the likelihood of shorts or of relatively thin dielectric regions in the dielectric). Additionally, the cathode or counter electrode materials (e.g., MnO₂ or polypyrrole or the like) typically used in SEC also exhibit self healing properties in that they tend to convert to more insulating materials when subjected to Joule heating resulting from localized dielectric failure or increasing localized current, thereby “healing” the region around the dielectric flaw.⁵ MLCC do not benefit from these factors. Because of these factors, t_{MLCC} is relatively high compared to t_{SEC} .

As discussed above the dielectric used in high VE_C MLCC (typically BT-based) exhibits relatively high ϵ' values, the breakdown fields (BDF) of these dielectrics is relatively low compared to BDF values for SEC dielectrics. For instance, a state of the art (SoTA) BT-based base metal electrode (BME) X5R MLCC can exhibit BDF of about 150 V/ μm while electroformed Ta_2O_5 -based dielectric in SoTA SEC has a characteristic BDF in excess of about 550 V/ μm , approximately 3.7 times the BDF of high VE_C MLCC dielectric. These data are for commercially available SoTA capacitors. Theoretical values for these dielectrics are as much as almost an order of magnitude higher in the case of BT.⁶

It is not enough to have high breakdown field. The insulation resistance of the dielectric must be adequately maintained over the life of the capacitor device. Thus, a more appropriate property, application design field (ξ , in V/ μm) should be used in comparing dielectric systems. From this value, the design dielectric thickness (t_ξ) for the voltage of interest is derived. In the case of tantalum pentoxide-based dielectrics, the design application field is typically on the order of ~160 V/ μm , whereas the value for BT-based X5R MLCC is on the order of ~10 V/ μm due, at least in part, to the processing method used to fabricate the MLCC structure as discussed above. Assuming these values are constant with respect to operating voltage and dielectric thickness (they are not, but are assumed to be so for this study), this means that in order to achieve a 6.3 V rating, t_{SEC} and t_{MLCC} need to be on the order of 0.04 μm (25 nm) and 0.63 μm (630 nm) respectively in order to achieve a capacitor that is

suitably reliable. Since the ϵ'_{SEC} is only ~ 27 while $\epsilon'_{MLCC(X5R)}$ is on the order of 3,000-3,500, it appears that MLCC have ~ 7 to ~ 8 fold advantage over Ta₂O₅-based SEC based on the ϵ'/t_{ξ} relationship. As mentioned above, however, ϵ' for BT-based dielectrics tends to reduce as t is reduced. This could reduce the ~ 7 to ~ 8 fold advantage of BT-based materials with regard to ϵ'/t_{ξ} . Additionally, ξ is dependent not only on materials processing, but upon flaw size and distribution as well. If ξ can be increased significantly for either system, VE_C would increase accordingly. This is a major focus of capacitor developers for MLCC, SEC and other capacitors.

Overlap area (A) needs to be considered as well. The overlap area per unit volume (A/V_A , where V_A is the active volume of the capacitor, electrodes included) needs to be considered. A typical (3216 100 uF X5R design) SoTA MLCC has an overlap area of $\sim 3500 \text{ cm}^2/\text{cm}^3$ for the entire device, or an A/V_A value of about $5,600 \text{ cm}^2/\text{cm}^3$ when discounting inactive volume of the MLCC device. A typical A case tantalum anode made with 150,000 $\mu\text{F-V/g}$ powder and intended for 100 μF target capacitance has an overlap area on the order of $\sim 65,000 \text{ cm}^2/\text{cm}^3$ when sintered. This ~ 12 to $1 A_{SEC}/A_{MLCC}$ ratio is a very significant factor in favor of SEC.

Finally, packaging efficiency (PE_C) must be considered. For this discussion, PE_C is the volume of the active portion of the device (electrodes included) as a portion of the total volume of the device. Standard design SEC have relatively poor PE_C , on the order of $\sim 10\%$ - 11% for an A (3216 or 1206) case size, while newer face down designs offer about double the PE_C or about 20-25% for an A case size.⁷ A SoTA 3216 (1206) case MLCC has a PE_C on the order of $\sim 60\%$ ($\sim 48\%$ excluding internal electrodes as a part of the active volume). The PE_C advantage clearly goes to MLCC with a PE_{CMLCC}/PE_{CSEC} being on the order of 3 to 6 better than for SEC depending upon the SEC type used as the basis for comparison.

Combining all of the above factors, the VE_C relation is

$$VE_C = PE_C \cdot \epsilon_0 \cdot \frac{\epsilon'}{t_{\xi}} \cdot \frac{A}{V_A}$$

where:

VE_C = Capacitance volumetric efficiency (F/m³)

PE_C = Packaging efficiency = (V_A/V_D)

ϵ_0 = Dielectric permittivity of free space 8.854×10^{-12} (F/m)

ϵ' = relative dielectric constant of dielectric

A = overlap area (m²)

V = V_D = Total device volume (m³)

V_A = Volume containing active portion of capacitor, internal electrodes included (m³)

This relationship may be further simplified, by removing the constant ϵ_0 , to become a figure of merit (FoM) relationship for comparison of different types of capacitors with respect to volumetric efficiency

$$FoM_{VE_C} = PE_C \cdot \frac{\epsilon'}{t_{\xi}} \cdot \frac{A}{V_A}$$

where:

FoM_{VE_C} = Figure of Merit for volumetric efficiency of capacitance

Using this relationship, it is possible to compare the volumetric efficiency capabilities of MLCC and SEC using the ratios noted above, as indicated in Table 1. Interestingly, although each capacitor type uses different routes to achieve high VE_C , both capacitor types exhibit somewhat similar FoM_{VE_C} and VE_C numbers. Advanced MLCC (0603 22 uF) and SEC (face down) are within $\sim 30\%$ of each other while the less advanced SoTA designs are within $\sim 25\%$ of each other. Relatively small increases in PE_C (e.g., from $\sim 22\%$ for face down design to $\sim 27.5\%$) for the tantalum devices should bring them back to parity with MLCC.

Table 1. Capacitance volumetric efficiency comparison of BT-based MLCC and Ta SEC

Capacitor Type	PE _C	ε'/t _ξ (V/μm)	A/V _A (cm ² /cm ³)	FoM _{VE_C}	VE _C (μF/cm ³)
MLCC (SoTA X5R BME (1206 100 uF, 6.3V))	0.61	3,977	5,651	1.38E+07	1.22E+04
MLCC (Adv SoTA X5R BME (0603 22 uF, 4V))	0.56	5,385	8,130	2.44E+07	2.16E+04
SEC (SoTA Ta 100 uF A Case, 4V)	0.12	1,363	65,000	1.06E+07	9.41E+03
SEC (SoTA Ta 100 uF A Case Face down, 4V)	0.22	1,363	65,000	1.95E+07	1.73E+04
Theoretical Hybrid Capacitor (1206 4V) ("Best of the Best")	0.61	5,385	65,000	2.15E+08	1.90E+05

Discussion

Perhaps the more important aspect of this exercise is to determine whether or not it would be possible to combine the “best of the best” of each of these types of capacitors to make a hybrid version of the two with the goal of achieving very high VE_C. Table 1 indicates that it should be theoretically possible to increase VE_C more than an order of magnitude by combining the best capabilities of PE_C and ε'/t_ξ for MLCC with the best capabilities of A/V_A characteristic of the most capable SEC. But how can this be accomplished? Significant research has been dedicated to maximizing the combination of ε'/t_ξ in combination with maximizing A/V_A, but these efforts to achieve this “holy grail” of the capacitor world have not met with a great deal of commercial success.^{8,9,10,11} Most of the methods used to date have involved application of a high ε' dielectric film to a high A/V_A substrate (typically a pressed and sintered porous cylinder or the like). Various forms of deposition such as dipping in sol gel precursors, electrochemical formation, or hydrothermal formation have been attempted. However, these systems typically exhibit very high leakage current while exhibiting only limited, if any improvement in VE_C over traditional SEC capacitors.

A concept under development at KEMET¹², is to deposit a thin film of high ε'/t_ξ on the high A/V_A substrates utilizing thin film coating techniques to cover the majority of the high A/V_A valve conductor substrate (the “anode”). Additionally, the substrate is post formed electrolytically to create an insulating dielectric film after establishing the high ε'/t_ξ dielectric film. The resulting insulating film is a composite of BT-based dielectric and valve metal insulator (Ta₂O₅ or the like). A representative internal structure is illustrated in figure 6. The post anodization process conditions and chemistry are carefully selected to minimize deleterious effects on the high ε' dielectric. The composite hybrid dielectric structure is intended to cover as much of the area of the valve conductor material (VC) as possible. However, it is understood that perfect coverage to establish a high resistance insulating film over the entire area of the substrate is likely not feasible with good yield. Thus, post anodization is used to form an insulating structure as illustrated in figure 6.

In forming the insulating hybrid dielectric film it is important to maintain a structure that is percolated by the high ε'/t_ξ material in order to maintain a high composite dielectric constant. If the post anodization formation is done in excess the anodization may “blanket” the high ε'/t_ξ material and effectively reduce the composite dielectric constant by ~2 orders of magnitude even with very low volume fractions of anodized valve insulator as indicated in figure 7. Additionally, it is very important to maintain phase purity in the high ε'/t_ξ material as well as to process it using methods that will not chemically reduce the high ε' dielectric to a less than ideal insulator without the possibility of re-oxidation later in the process.

Research at KEMET is focused upon establishing an optimized high ε'/t_ξ material coating on the VC substrate. Figure 8 illustrates progress thus far. The figure indicates that it is possible to coat a relatively high fraction of the VC substrate or more with the high ε'/t_ξ material. Materials selection is also a key factor in development. Initial development work indicates that phase pure, BT-based dielectric films may be achieved on NbO/Nb₂N-based substrate material as illustrated in figure 9.

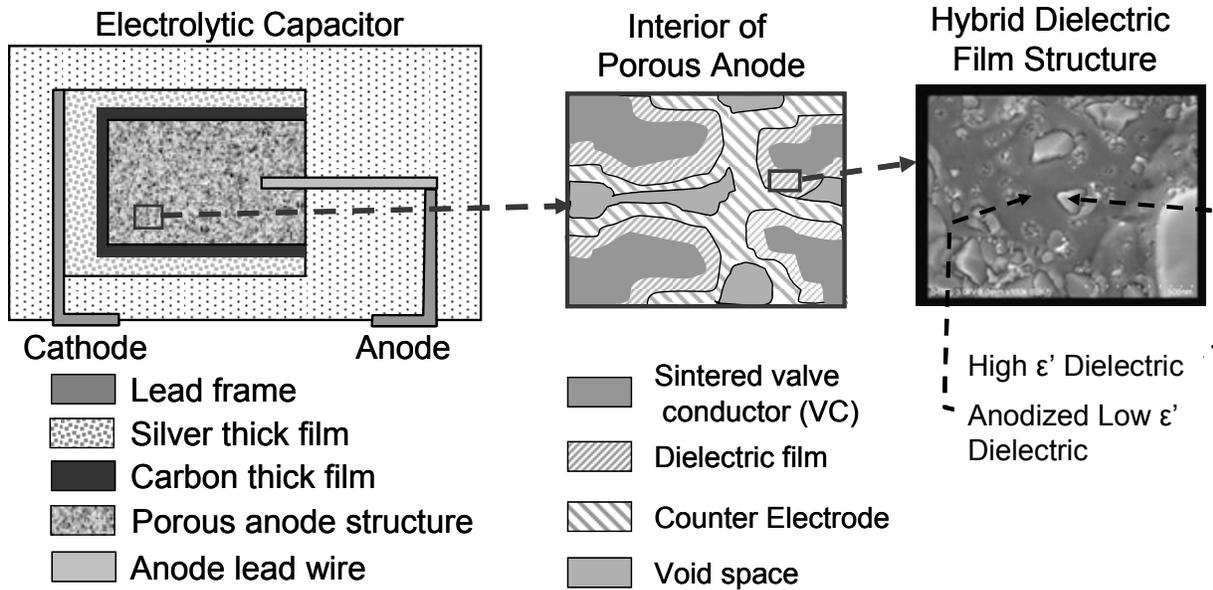


Figure 6. Structure of hybrid dielectric SEC capacitor

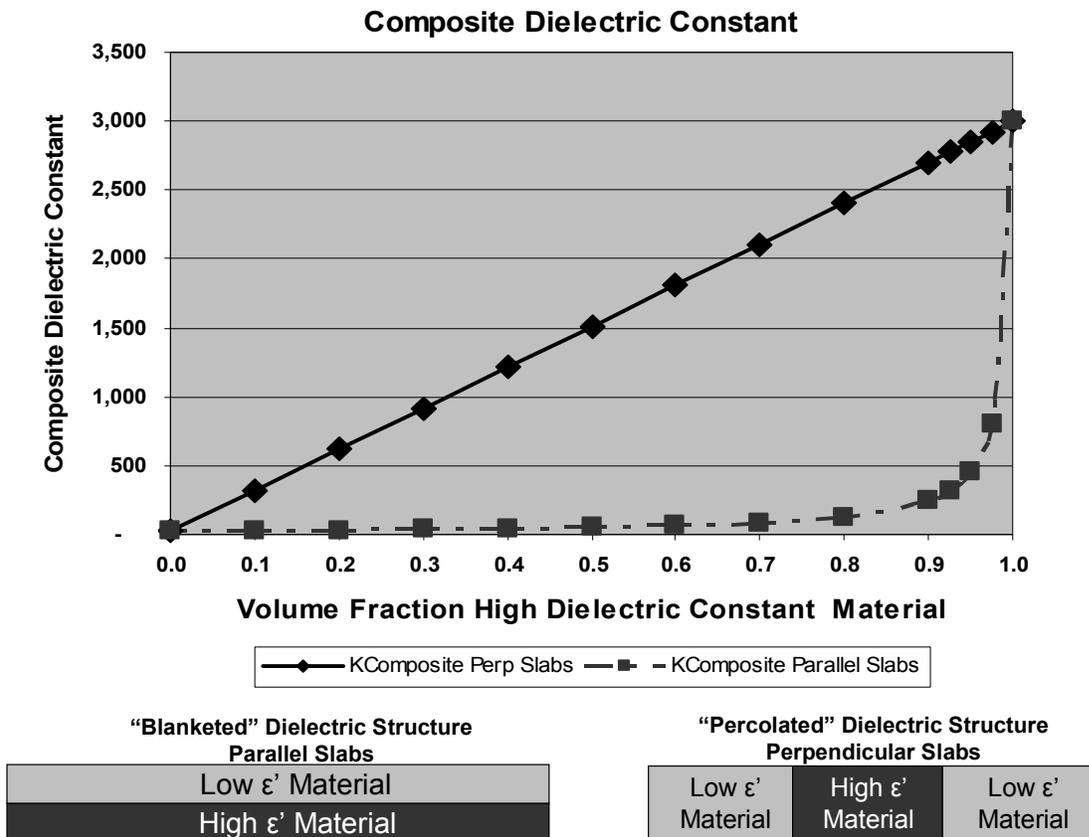


Figure 7. Composite dielectric constant of blanketed vs percolated hybrid composite structures

Pre-Anodized Hybrid Dielectric on Valve Conductor Structure

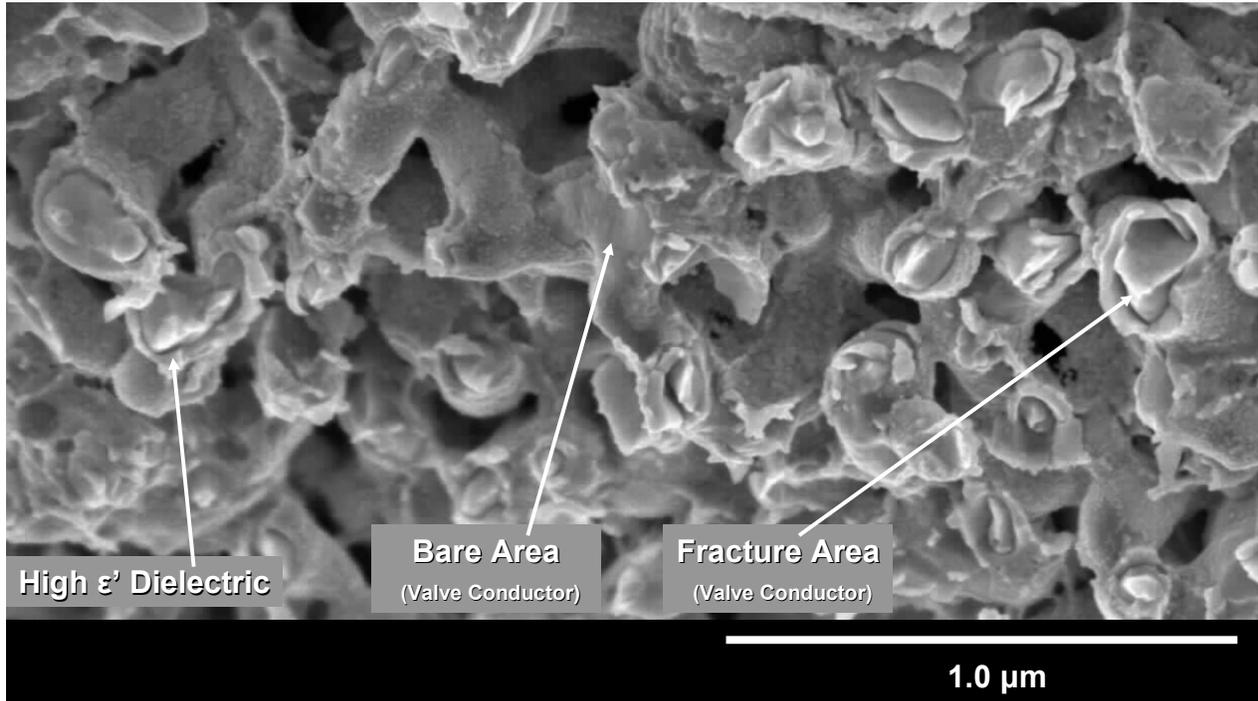


Figure 8. Representative high CV structure coated with high ϵ'/t_{ξ} material

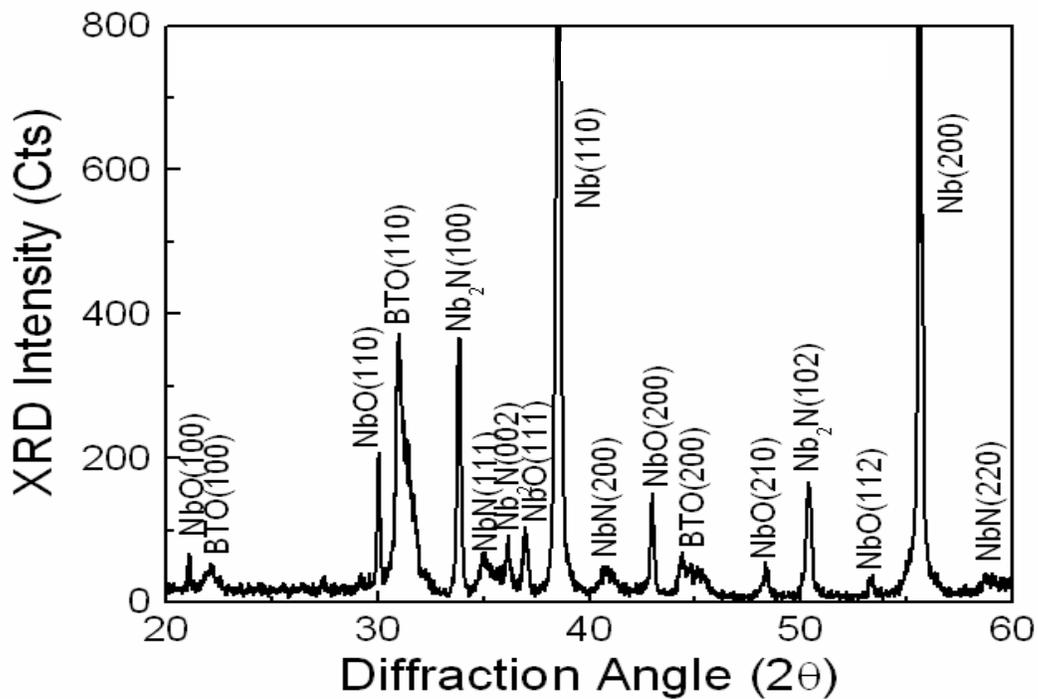


Figure 9. X-Ray diffractogram of dielectric on NbO substrate

The potential for increased capacitance for hybrid dielectric capacitors is illustrated in figure 10 in comparison to an A case sized 100 μF capacitor. The potential for advancement in VE_C is very significant with as much as an ~ 14 fold increase in VE_C being possible for the conditions modeled.

It is likely that actual increases will not be as large. Initial wet capacitor data (see figure 11) indicate that it is possible to more than double wet capacitance. This doubling in VE_C capability would be quite significant if commercially applicable to SoTA capacitors.

However, many challenges remain. The insulating properties of the hybrid dielectric devices need to be improved as the $\Omega\text{-F}$ product is $\sim 10\%$ that of the control as indicated in figure 12. Additionally, it would be prudent to focus development efforts upon increasing ϵ'/t_ξ to amplify the effect of the high dielectric constant of the high ϵ' portion of the dielectric composite as well as to maximize A/V_A by making the most efficient and effective use of the anode conductor volume (i.e., maximizing coatable surface area per unit volume in a coatable structure). Significant effort also needs to be focused on increasing PE_C of the SEC devices in order to make the best use of the high ϵ'/t_ξ materials combined with the high A/V_A structure. Finally these devices will likely have higher ESR and increased capacitance “roll off” with frequency compared to MLCC similarly to the situation described above for traditional SEC. Development efforts will also focus upon reducing these phenomena. It is likely that the form factor of the hybrid SEC device will need to be modified in order to do this. Structures that are potential candidates for high A/V_A combined with low ESR and cap roll off with frequency are illustrated in figure 12. It is likely that the hybrid dielectric will be applied to these types of substrate structures to address the above issues. While much development work remains, hybrid composite dielectrics show promise with respect to achieving very high VE_C potential in a relatively easy-to-manufacture capacitor system.

Summary

The rates of increase in capacitance and VE_C for MLCC and SEC have been impressive. Maximum capacitances available for MLCC have doubled about every 13-14 months, outpacing Moore’s Law for IC development. Hybrid dielectric VC electrolytic capacitors show promise for increasing the VE capability of start of the art capacitors. Much development is yet to be accomplished, however. A primary area of focus for development will be optimal selection of the VC material chemistry and VC powder physical properties. The optimization of the high ϵ'/t_ξ precursor formulation and delivery process to achieve uniform, thin and flaw free films of the high ϵ' dielectric will also be key to successful development as will the optimization of the anodization chemistry and process to minimize leakage current and the maximize $\Omega\text{-F}$ product. It will also be important to maximize the portion of the high ϵ' portion of the hybrid dielectric as well as to maximize ϵ'/t_ξ for that material.

Additionally, it will be important to optimize the counter electrode chemistry and process to achieve maximum coverage of the hybrid dielectric without ill effect. In order to achieve maximum effectiveness, the hybrid system needs to be developed to work with the highest A/V_A conductor systems. Moreover, the system should be compatible with future packaging systems that are developed to maximize PE_C so as to preserve or enhance the gains in VE_C realized from the complementary materials and substrate development activities described above. Using the hybrid dielectric system, it will be possible to manufacture capacitors with myriad structures with relatively simple and well established processes. These structures will likely include impregnation of complex, porous structures of various types that have been optimized for A/V_A as well as to reduce ESR and capacitance roll off with frequency and ESL.

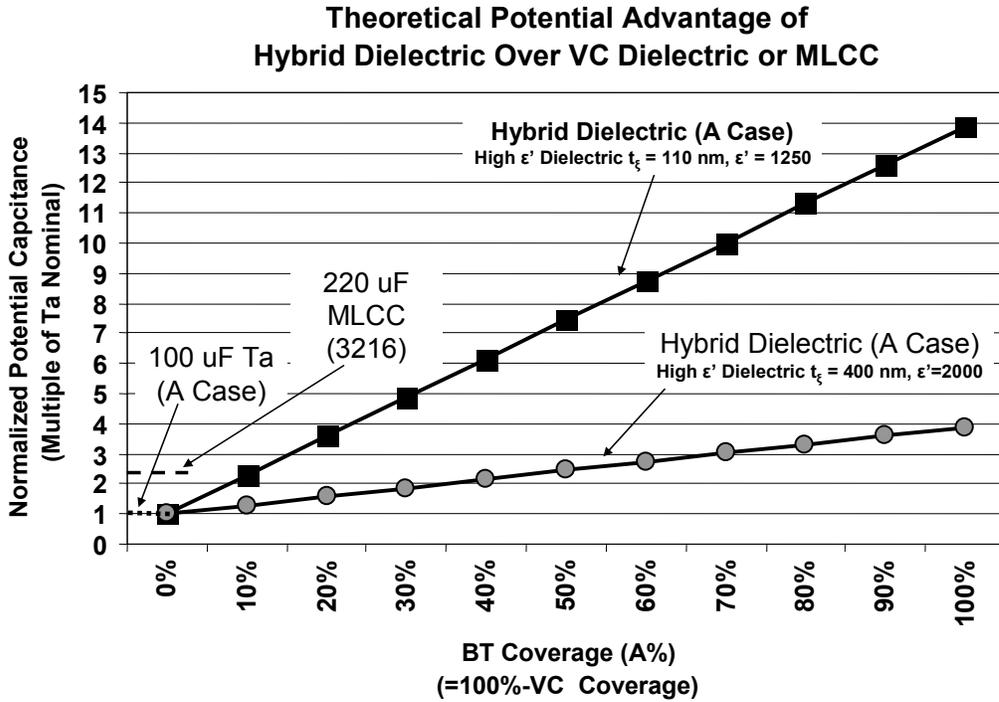


Figure 10. Potential V_{EC} for hybrid dielectric SEC

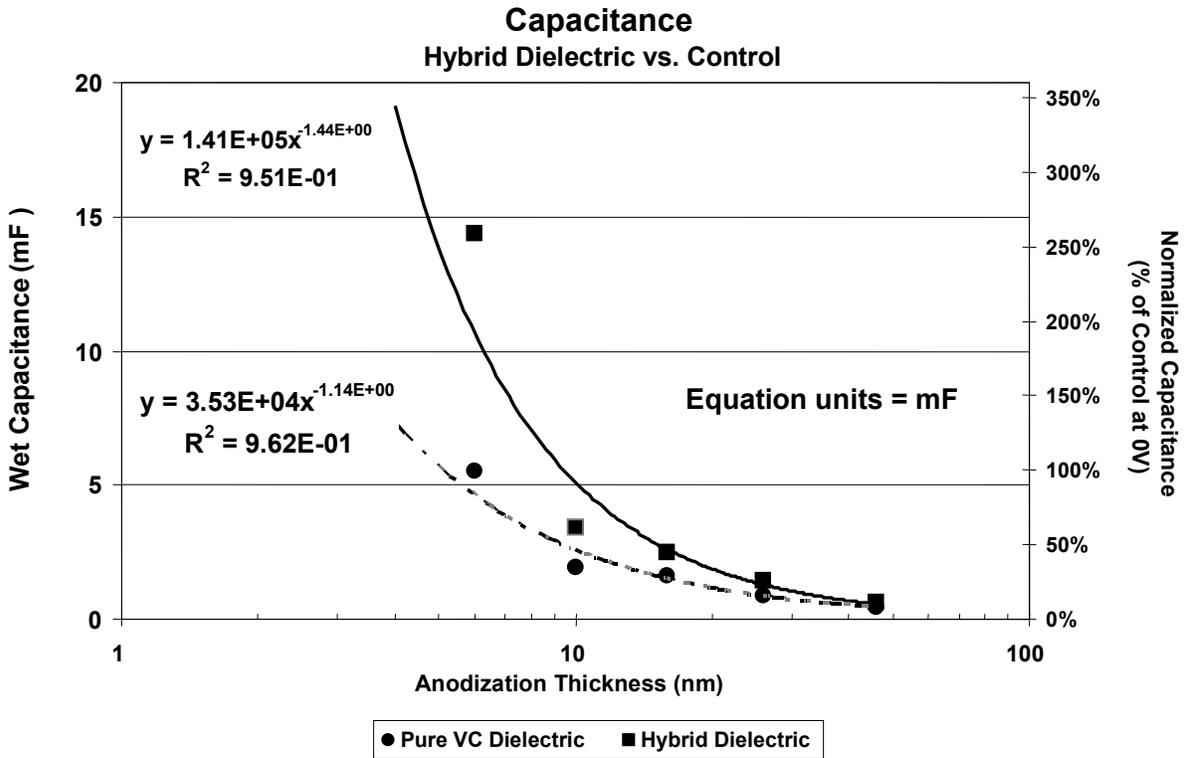


Figure 11. Wet capacitance comparison of control vs. hybrid SEC

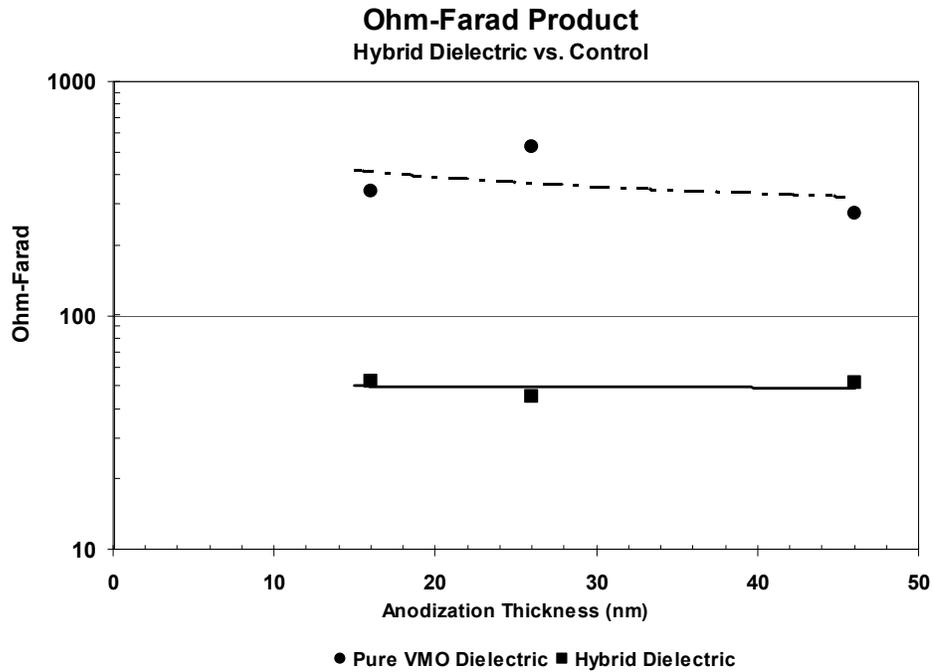


Figure 12. Wet Ohm-Farad product for control vs. hybrid SEC

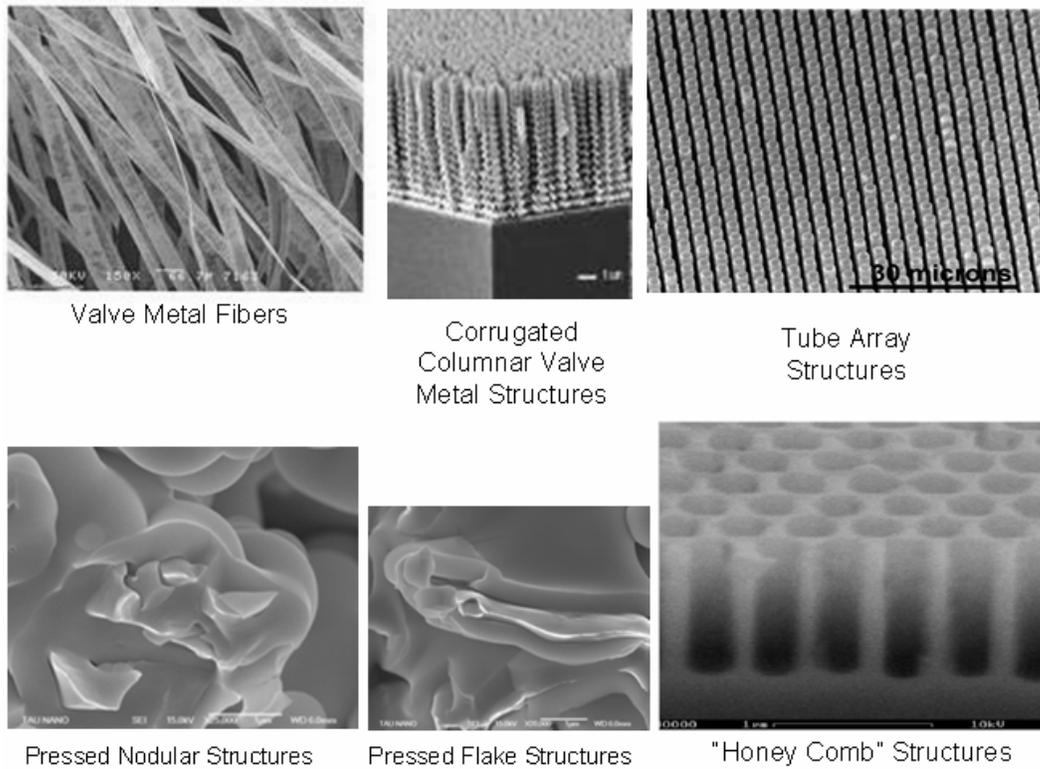


Figure 13. Porous microstructures targeted toward maximizing surface area per unit volume in an open pore structure

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