# ESD Susceptibility of Ceramic Multilayer Capacitors

by J. D. Prymak and J. Piper , (Retired) KEMET Corp.
Phil (F. L.) Stair, (Retired) FORD North Penn Electronics
KEMET Electronics Corp.
P. O. Box 5928
Greenville, SC 29606
(864) 963-6300 / FAX (864) 963-6322

## *ABSTRACT*

*Ceramic capacitor failures due to electrostatic discharge (ESD) surge voltage exposure has historically been discounted because of the huge over-voltage capabilities of this device. A part designed for 50 VDC application would typically break down between 800 and 1,500 VDC. This over-voltage capability was a subsequent benefit from the inability of manufacturers to effectively use thinner dielectrics. The 50 VDC dielectric was only slightly thinner than the 100 VDC design and the stress on the dielectric was proportionally weaker. Improvements in this aspect of the technology have moved the dielectrics to thinner dimensions that are equally stressed as the 100 VDC designs, and now have also allowed designs of 25 and 16 VDC rated components. This development has moved the breakdown voltages down in the realm of 400 VDC, allowing smaller chip designs and subsequently, a reduced safety factor for ESD failures.*

*Awareness of ESD damage to electronic components has caused manufacturers to adopt various methods of determining the ESD threshold (sensitivity) of individual components. Some of these methods were designed for a broad range of components and subjected capacitors to unrealistic stress levels not duplicated with other components, and highly unlikely to be experienced in a "real world" application. In this article we will examine the causes of unrealistic conditions and the capabilities of MLCs to withstand ESD as well as where we see problems for the MLC in future designs.*

## *Capacitor Design*

The thickness of the dielectric used in ceramic capacitors is determined by successfully achieving a required failure rate level through accelerated life testing. It has nothing to do with capacitance change with applied DC bias, but merely achieving that required quality level determined by long term exposure to high temperature and bias and achieving acceptable capacitance, dissipation factor (DF), and insulation resistance (IR) shifts. (The dissipation factor has become an additional concern with thinner dielectrics and this issue is being discussed by the various associations.)

Twelve or fifteen years ago the state of the art for dielectric formation was approximately 0.9 mils thickness. This was the dielectric thickness used for the lowest rated, or 50 VDC application. The 100 VDC design was typically 1.3 mils thickness. The stress for the 50 VDC design was then 56 V/mil compared to 77 V/mil for the 100 VDC design. The thickness of the dielectric was limited by materials and process capabilities used to achieve acceptable failure rates in accelerated life testing. Faults created in the dielectric during the manufacturing process became more detrimental to the thinner dielectric than the thicker designs, as they became a greater percentage of the whole thickness.

Subsequent material and process improvements have led to much thinner dielectric design. For the 50 VDC design, 0.7 mils is commonplace, with 0.5 mils thickness beginning to dominate new offerings. This trend supports, and at the same time, is accelerated by the drive for capacitor size reduction.

Regardless of minimum thickness capability, not all chips of a specific voltage rating and dielectric type may utilize that minimum thickness, even from the same manufacturer. Consider the 1206 chip. With 8 mil margins at the ends, and 6 mil margins on the sides, it has an effective area of 0.004992 square inches. For an X7R material with a dielectric constant (K) of 2500 and a thickness of 0.7 mils, there is approximately 4,000 pF capacitance per layer.

*Cap(*pF*) = 0.224 x Area x K x Eff / Thick*

As such, the minimum capacitance that could be designed using this thickness would be 4,000 pF; but this chip size offering for this voltage actually extends down into the realm of 680 pF to 1,000 pF. This is accomplished by reducing the capacitance per layer with thicker dielectric layers. To achieve 1,000 pF in a single layer, a thickness of 2.8 mils for this X7R is required. For reasons beyond the scope of this paper, very few capacitors are designed with a single effective (Layers - 1) layer and many cover layers. They are more likely limited to a minimum of three or five effective layers to achieve the minimum capacitance. If three layers are required, then the thickness becomes 8.4 mils. If this thickness were to be stressed to the same level as the 0.7 mils at 50 VDC, it would require 600 VDC.

This increased thickness also increases the breakdown levels (though not in a straight linear fashion as the stress level) as the capacitance value decreases. Regardless of the difference in design and decreased stress level, this chip is still marked, tested, and delivered as a 50 VDC part.

These changes in design are extremely important considerations in understanding ceramic capacitors and their successful history with ESD capabilities.

## ***ESD Test and Testers***

A current calibrated ESD simulator was incorporated, in this investigation to apply voltage pulses to the capacitors under test. An Electro-Tech Systems (ETS) Model 910 simulator was used with capability of positive and negative pulses applied at intervals between 0.5 seconds and 10 seconds. Peak voltage capability was 8,000 volts.

For this test, the standard condition for component evaluation was 5 positive pulses, followed by 5 negative pulses. Capacitance, DF and IR were measured initially and post test. Voltage levels were increased until a shift in post test measurements were noted. Once a predetermined shift selected by the customer was met, this voltage became the ESD threshold for that device.

The simulator is designed to duplicate the condition of a component being subjected to a sudden high voltage discharge. We have all experienced uncomfortable ESD effects when we walk across a carpet in a dry atmosphere and then touch a conducting object releasing the charge built-up in our bodies. Under specific conditions, a spark may also be observed. It is this type of discharge, now standardized as the "human model," that causes much of the concern for the ESD susceptibility of electronic circuits. Our bodies act as a capacitor that builds up a charge until it is discharged to ground.

The simulator can duplicate the *human body model* as well as *machine models* (discharging from a mechanical source). The *human body model* provides a 150 pF charge capacitor and a 1,500 ohms series resistance that it discharges through. The *machine model* has a 200 pF charge capacitance and no series resistance.

A charging capacitor is connected to a high voltage power supply to charge it. The charge capacitor is then disconnected from the power supply and connected to the device under test. The charge is transferred to the device through the series resistance and there is energy dissipated through it. This loss of energy is why conservation of charge instead of conservation of energy is used in analyzing this test.

Though the typical voltage levels for the *human body model* is given as 8,000 volts, and *machine model* given as 2,000 volts, these levels may be too high for some circuit evaluations. In many cases, the different users may define their own variations on these tests or categorize the susceptibility to different levels. A typical requirement may specify a 2,000 VDC *human body model* discharge pulse, and a 200 VDC *machine model* discharge pulse. These requirements were defined as maximum capability of the semiconductor devices in the circuit, and since these capacitors are used in conjunction with these devices, the pulse requirements are the same.

## ***Conservation of Charge***

A capacitor presents an unusual situation for the ESD investigation. The original charge ($Q_C$) in the charging capacitor ($C_C$) is subsequently split between this capacitor and the capacitor under test ($C_{CUT}$). Ideally, the original charge ($Q_C$) is the product of the capacitance and the voltage (expressed in coulombs) as:

$$Q_C = C_C \times V_T$$

where $C_C$ is the capacitance of the charging capacitor and $V_T$ is the voltage to which it was charged. Connecting the test capacitor causes the charge to now be supported by two capacitors at a new voltage ($V_F$):

$$Q_C = (C_C + C_{CUT}) \times V_F$$

where $C_{CUT}$ is the capacitance of the capacitor under test and $V_F$ is the common final voltage across each of the capacitors. The charge remains constant and the voltage changes by the ratio of $C_C$ to ($C_C + C_{CUT}$). If $C_{CUT}$ is insignificant to $C_C$, then the voltage changes very little, whereas if $C_{CUT}$ is significant to $C_C$, then the voltage changes dramatically. As an example, if $C_{CUT}$ is the same as $C_C$, then the final voltage ($V_F$) is half the original ($\frac{1}{2}V_T$). If $C_{CUT}$ is 1/20th of $C_C$, then the final voltage is ~95% of the original, and if $C_{CUT}$ is 20 times $C_C$, then the final voltage is ~5% of the original.

It is important to see that as the capacitor under test decreases in value, the subsequent voltage across it increases. The common manufacturing practice of using thicker dielectrics for smaller capacitance values in a given case size and dielectric, diminishes the susceptibility of the smaller cap values to this test as they obtain increasing breakdowns levels with increasing thickness.

It is also important to realize from the description of the various models for ESD simulation, the source capacitance that is charged is relatively small compared to the normal capacitance values of the 1206 X7R chip.

## ***Multiple Pulses***

In some cases, ESD testing has adopted one of the common axioms of testing: that if a device must withstand any single experience, it should be tested to many of these experiences to establish credibility. In this light, multiple ESD pulse exposures (both positive and negative) are often utilized to establish ESD capability. The problem with this multiple application that is unique to capacitors is that the capacitors store charge cumulatively. If no conditions are included to allow the capacitor to discharge between pulses, the cumulative charge results in ever increasing voltages. If the cumulative ESD voltage is high enough with no discharge between pulses, it is only a matter of the capacitance and breakdown capability of the CUT, and the number of pulses attempted before the dielectric breakdown level is achieved and the capacitor fails. Many ESD simulators have programming capabilities for adjusting intervals between pulses as well as the number of pulses; and yet in the same standard offerings, make no provisions for discharge of the device under test, between pulses.

The following table shows the voltages developed across an ideal capacitor subjected to multiple 8 kV pulses from an ESD simulator with the *human body model* discharge network. The series resistance is insignificant in this calculation due to charge transfer, and the assumption is that no charge is lost between pulses due to the extremely high insulation resistance of these devices.

***Table I Voltage Build-Up - Ideal Capacitor***

| Cap (nFd) | 1 Pulse | 2 Pulses | 3 Pulses | 4 Pulses | 5 Pulses |
|---|---|---|---|---|---|
| 100 | 12 | 27 | 36 | 48 | 60 |
| 33 | 36 | 72 | 108 | 144 | 179 |
| 10 | 118 | 235 | 349 | 463 | 574 |
| 3.3 | 348 | 681 | 999 | 1,303 | 1,594 |
| 1 | 1,043 | 1,951 | 2,740 | 3,426 | 4,023 |

The range of values for the preceding table reflects the range of capacitance typical in a 50 volt rated X7R, 1206 style chip, surface mount capacitor. Note that these results were calculated for ideal capacitors, or NP0/C0G types, and the effect of the voltage coefficient of capacitance present in X7R or Y5V capacitors has not yet been considered.

Dielectric breakdown voltages (BDV) for MLCs are typically in the range of 500 to 1500 volts, which are readily exceeded with multiple pulses, especially in CUTs with low values of capacitance.

## ***Natural Spark Gap***

During the testing in our lab using multiple pulses, it was noted that the chips could be heard discharging after a number of pulses. These

discharges could also be visually observed as arcing over the top surface on some of the chips. Based on the spacing between the silver termination lands on the chips of ~ 65 mils, and the 75 kV/inch[3] air discharge rule, a voltage of less than 4.8 kV was being attained to cause this discharge. The 75 kV/inch applies to air spacing whereas the chip has some field its field enhanced by the dielectric, resulting in a lower breakdown voltage of uncertain magnitude.

In any event, these discharges were an experimental indication of much higher voltage appearing across the chip's terminals, higher than any calculated that we made for the "ideal" type capacitor.

This air-discharge was not noted at both locations. This leads us to conclude that the natural spark discharge attainable with this device is as indeterminate as any spark discharge device. It is too highly dependent on atmospheric conditions, geometry and external elements to be relied upon to protect the device in higher voltage states. Even adding a spark discharge gap in the circuit design would eliminate some of the geometry variations, but would still be open to the others.

## *Bleeder Resistance*

It was determined that a modification was necessary, in order to avoid charge accumulation during multiple pulse testing of the CUT. One method would be to manually discharge the part between pulses, but this interrupts the timing of the pulse application. We have found that inserting a high value resistor in parallel with the CUT is a simple, but effective, way to achieve discharge. The resistance value selected had to provide a long RC time constant compared to the ESD pulse, but short compared to the pulse interval. in our investigation we decided to use a 10 Megohms resistor .

***Figure 1. Measured Voltage Coefficient***

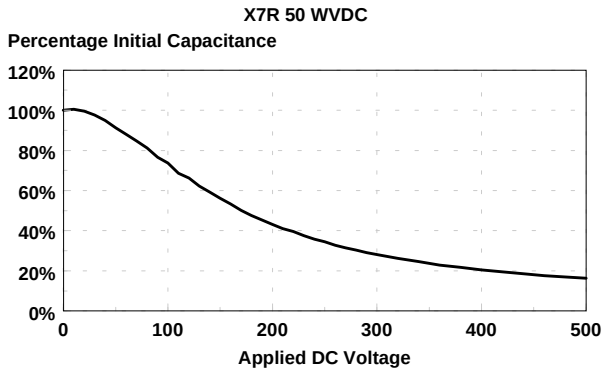
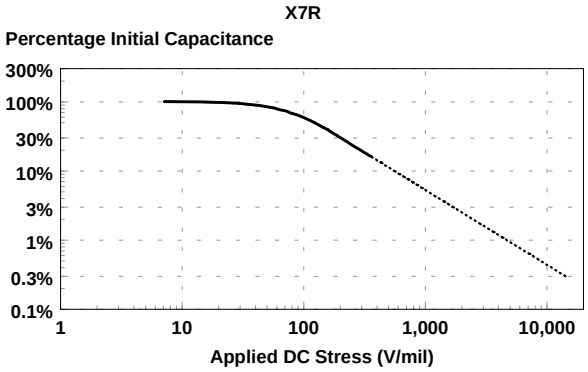



***Figure 2. Voltage Stress Extrapolated***

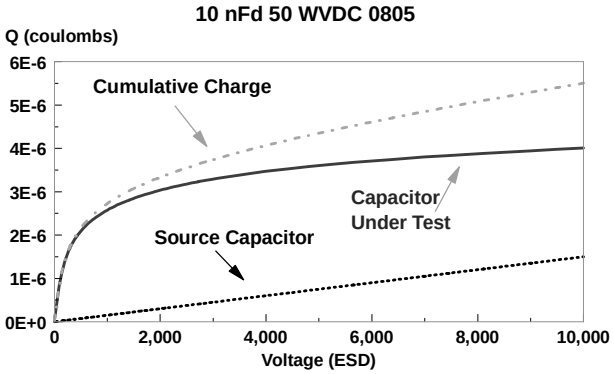



## *Voltage Coefficient of Capacitance*

As previously mentioned, the capacitance values in Table I are typical of X7R capacitors. However, the capacitance of X7R MLCs is highly dependent upon applied voltage as shown in Figure 1. The applied field causes a slight increase in capacitance and then a steady decay. We tested this part through 500 VDC, but this was not sufficient to project the capacitance changes with the voltages that were building up across the capacitor. Figure 2 is another view of the data with an extrapolation out past 500 VDC. By utilizing the logarithmic scale, a nearly linear interpretation is revealed. By plotting stress instead of the bias, this effect can be applied to any unit of this X7R material, regardless of thickness.

From Figure 1 and 2, it is readily seen that as the voltage on the capacitor increases, less capacitance is available to absorb the ESD charge. Now

***Figure 3. Cumulative Charges***



instead of the ideal relationship where the charge is calculated as:

$$Q = C \times V$$

we must consider the voltage dependence of the capacitance and use the relationship:

$$Q(v) = \int_{v} C(v) \times dv$$

Using the capacitance-voltage relationship from the measured data (Figure 2) and then integrating, we obtain the charge retained by the CUT for any given voltage. Since the charging capacitor and CUT pair achieve the same voltage once they are coupled, the resulting summary charge of the CUT and the charge capacitor can be calculated for all voltages through the ESD voltage. The graph in Figure 3 illustrates these combined and individual effects for a 10 nF capacitor tested with a source capacitance of 150 pF, through 10 kV.

Using the conservation of charge, the charge capacitor and CUT will combine to a summary charge after each pulse. We can deduce the voltage required for this pair to achieve the summary charge from Figure 3, and thus predict the voltage after each pulse. Keep in mind that as the charging capacitor is removed from the circuit, it removes some of the cumulative charge. If enough pulses are applied and the CUT attains the same voltage as the charging capacitor, there is no voltage increase and all subsequent pulses achieve the same cumulative charge.

Using the same inputs as used previously, Table I must be dramatically modified for typical X7R capacitors to the values in Table II. Notice that for the 1 nF capacitor after 4 pulses, no additional number of pulses will result in a voltage greater than the source capacitor voltage of 8,000 volts.

**Table II Voltage Build-Up - X7R Capacitors**

| Cap (nF) | 1 Pulse | 2 Pulses | 3 Pulses | 4 Pulses | 5 Pulses |
|---|---|---|---|---|---|
| 100 | 11 | 22 | 34 | 46 | 59 |
| 33 | 36 | 76 | 124 | 188 | 280 |
| 10 | 141 | 523 | 1,744 | 4,015 | 6,101 |
| 3.3 | 1,329 | 2,708 | 7,584 | 7,934 | 7,989 |
| 1 | 5,316 | 7,828 | 7,990 | 8,000 | 8,000 |

## *Measured Voltages*

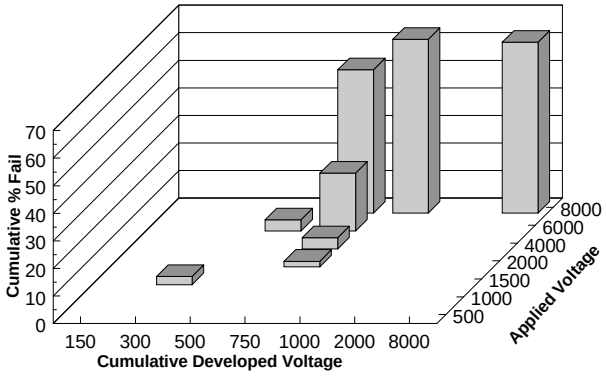
The dramatic effect of considering the voltage coefficient of capacitance of the CUT was checked experimentally using a Keithley electrometer (Model 619). The electrometer had an input impedance of 2 x $10^{14}$ ohms shunted by 20 pF of capacitance. We estimated that the cable and connectors contribute another 10 pF of capacitance.

A 1.0 nF chip capacitor with a voltage coefficient of capacitance of -50% at 500V and a dielectric thickness of 2.4 mils was used. It was subjected to a 5 kV pulse from a 100 pF charging capacitor. Using the electrometer to measure the CUT adds the additional capacitance from the leads and meter input to the capacitor, thus diminishing the resulting voltage. Without the electrometer the calculated voltage after the pulse is 589V. With the extra 30 pF of capacitance from the electrometer added as it is attached to test the CUT, the calculated number was 554V and we measured 540V. The calculated value assuming an ideal capacitor is 442V, and this is well surpassed because of the voltage coefficient of capacitance effects.

Another X7R capacitor was tested, this time a 1 nF capacitor with a dielectric thickness of 1.4 mils and a voltage coefficient of capacitance of -70% at 500V. The predicted voltage without the electrometer in the circuit is 913V. With the electrometer the calculated voltage is 785V. Again, the ideal capacitor voltage calculation gives 442V. The measured value was 780V, in very good agreement with the model including the voltage coefficient effect.

## *Experimental Results*

***Figure 4. Cumulative Failures - 1,000 Pieces***



Approximately 1,000 capacitors, either 0805 1,000 pF X7R or 1206 10,000 pF X7R units, were ESD tested. The test techniques used either the human model with a 150 pF charging capacitor and a 1500 ohm series resistor or the machine model with a 200 pF charging capacitor and no series resistor. Between 1 and 5 pulses were applied. Different tests were conducted with and without a bleed resistor of 10 Megohm in parallel with the capacitor under test. Some tests conducted without a resistor, were shorted between pulses.

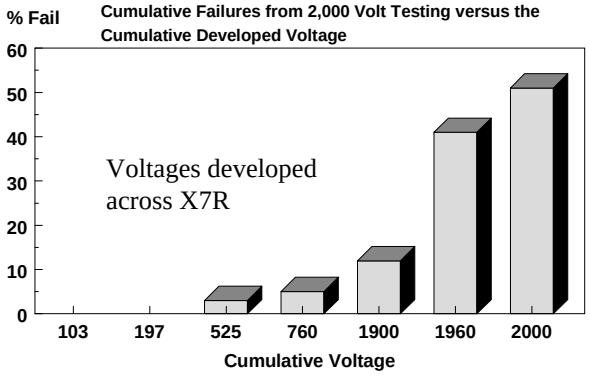
In early experiments we observed occasional air discharge around the capacitor after the second or third of multiple ESD pulses, depending on the capacitance value. This indicated that the capacitor had charged to a very high voltage and led to exploration of the effect of physically discharging the test capacitor between pulses. The discharging or avoidance of cumulative charge from multiple discharges resulted in the observation that the failure rate was greatly reduced. Figure 4, therefore, presents the failure rate data in a matrix of the applied ESD pulse voltage and the maximum voltage derived from the accumulated charge as discussed earlier. Cells in which 10 or more capacitors were tested are shown on the chart. A failure was defined as a capacitor not meeting initial insulation resistance criteria. Figure 5 shows the failure rate versus estimated cumulative voltage as a result of 2000 volt pulses. These capacitors have an ultimate breakdown voltage (i.e. under a slow voltage ramp) of about 1000 volts.

The test results did not show a significant difference in failure rate between the machine model (no series resistance) and the human model (1500 ohm series resistance), thus the results for the two sets of tests were combined to obtain Figures 4 and 5. In Figure 5 the 1900 and 2000 volt results came from human model tests; the 1960 volt result came from the machine model.

We were also unable to distinguish between the performance of 10,000 pF capacitors and 1,000 pF parts when compared on the basis of the same cumulative voltage. Obviously, under the same test conditions the 10,000 pF parts attained lower cumulative voltages, and so only a very few failures occurred.

## ***Future Designs and Susceptibility***

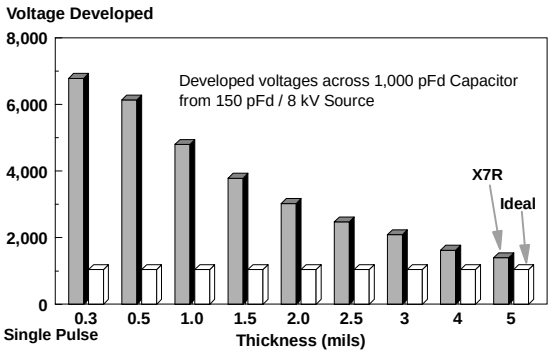
***Figure 5. %Fail versus Developed Voltage***




The direction of the industry is down-sizing. Same values but smaller chip sizes. The 1206 X7R that had to use the very thick dielectric design to achieve 1,000 pF, can be built with thinner dielectrics in 0805, 0603, and 0402 chip sizes. Since the effective area decreases appreciably with the smaller chip sizes, the capacitance per layer is much lower for the thinner dielectrics as the size decreases. For instance, to build the same 1,000 pF in an 0805 chip, dielectric thickness of 4.4 mils is sufficient, 1.6 mils for an 0603 and 0.5 mils for and 0402. Hand-in-hand with decreasing the sheet thickness is a parallel program aimed at increasing the dielectric constant of the X7R to 5000, or twice that of the previous designs. This would help the ESD capability as it would almost double the minimum thickness in the 1,000 pF designs - but not enough.

The discussions in this paper have really centered on the X7R dielectric, the most popular. There have been few reported problems with NP0 or the C0G dielectric because it is generally found to be a stronger dielectric than the X7R, but again with down-sizing, the lower capacitance values will no longer have the multiple thicknesses

***Figure 6. Pulse Voltage Developed vs Thickness***



associated with the larger chip sizes. The larger voltages required for failure in these devices might not be realized with these devices as they may discharge externally.

The high capacitance dielectrics of Y5V and Z5U are no longer immune to this potential damage as well. In the 0805 and 1206 realm, their capacitance values were again so high as to result in little charge build up. Smaller chip sizes and smaller capacitance values along with increased voltage coefficients will also result in new failures associated with down-sizing.

## Downsizing

Looking at the 1,000 pF capacitance unit, we see what happens as we down--size by using thinner dielectrics with a known voltage coefficient. The gray bars in the graph in Figure 6 illustrates the first pulse voltage developed across the X7R 1,000 pF capacitor from a *human body model* simulator with a discharge pulse of 8 kV. These voltages are those developed using the previously studied X7R for various dielectric thicknesses (in mils). The open bars represent that voltage of 1,042 built up across an "ideal" capacitor with no voltage coefficients, such as the NP0 or C0G ceramic.

## Discussion

The ESD tests which were carried out in 3 groups at two laboratories were designed simply to gauge ESD sensitivity and not to focus on specific potential correlation. The strong relationship between failure rate and cumulative voltage on the capacitor quickly became evident. The importance of including the voltage coefficient of capacitance in estimating cumulative voltage was also shown.

A major weakness in this work is in the identification of "failure". We use the common definition of a decrease in insulation resistance based on our initial requirements. Parts we considered "good" were not evaluated for degradation of parameters such as load humidity test performance or thermal shock sensitivity, which may have been compromised by the rapid application of a high voltage.

Published data on piezoelectric properties of barium titanate ceramics[1,7] predict that stresses of the order of the bulk modulus of rupture are generated with about 12V/um voltage stress or about 300 - 400 volts on capacitors of the design used here. An influence of charging rate on breakdown voltage values of MLCs has also been noted.[4]

The results here and the cited publications suggest caution when exposing MLCs to voltages high compared to their rating from any source.

## Acknowledgment:

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