HIGH VOLTAGE CONSIDERATIONS WITH MLCs

M. Prevallet, S. Bagdy, J. Prymak, M. Randall
KEMET Electronics Corp., PO Box 5928
Greenville, SC, USA 29650

Abstract

Mica and film capacitors dominate most of the high voltage applications. The combination of high voltage withstanding characteristics and their stability under most electrical and environmental stress conditions have favored these types of capacitors in many designs. Over the years, ceramic capacitors have been developed for high voltage applications that have been proven very reliable in these applications, but the early presentations of this product involved variations on the disk capacitor design.

The traditional MLC (multilayer ceramic) capacitor has dominated low voltage applications (<500 VDC) but continues to encroach into the high voltage applications beyond 500V through 10kV. These applications include multiplier circuits, high voltage fly-back power supplies, high-energy pulse circuits, snubber applications, radar, etc.

I. CERAMIC HIGH VOLTAGE DISK

Traditional high voltage disk capacitor configurations have required relatively thick single layer dielectric structures (2 to 10 mm), as well as special treatment of the outer edges of the dielectric disk to suppress arc-over.

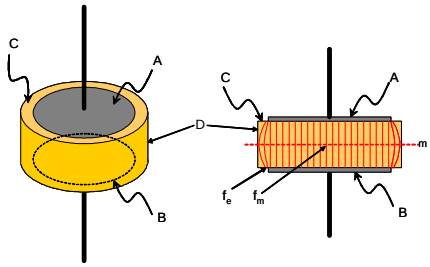

Figure 1. Pressed ceramic disk, leaded capacitor.

In the disk type capacitor, the overlap areas of the conductive plates are contained within the pattern areas of the plates themselves. In Fig. 1, the perspective view of this capacitor type is shown on the left and a cutaway view is shown on the right. The top electrode (A) exists within a circular pattern that is concentrically placed inside the top circular area (C) of the fired ceramic pellet (D). This pattern is duplicated on the bottom surface with a second electrode (B). An electric field exists between these plates as they are charged, with a relatively uniform electric field (fm) within the center depth (m) area of the disk. The electric field lines "bulge" out of the electrode overlap, near the outer edges of the pattern, resulting in an increase in the electric field intensity near the outer edge of the plates (fe). By keeping the plate patterns (A and B) inside of the area defined by the diameter of the disk, these high fields and their associated high charge concentrations are kept away from the vertical outer surface of the dielectric, improving high voltage performance.

The leads are attached with solder to the plate areas allowing this structure to be utilized in an electrical circuit. Again, this is normally coated with some type of epoxy or insulative material to help suppress the arc-over. The coating also prevents contamination of the edge, which could degrade the insulative nature of the dielectric.

In the past, designers have also used special configurations in order to maximize high voltage performance. Some designs have incorporated machined or hollowed-out surfaces, which depress the plate areas below a flanged collar. This is to afford the outer edge of the ceramic additional protection against arc-over. This design is typically referred to as "door-knob" design as the machined assembly is large with rounded edges and looks like a doorknob. These designs enable rated voltages in excess of 50kV.

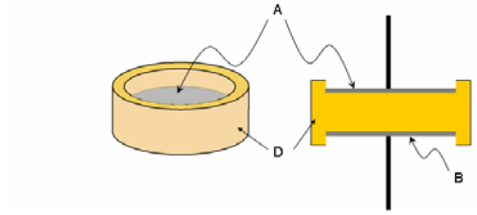

Figure 2. "Doorknob" structure for ceramic high voltage.

While disk capacitors are valuable for very high voltage applications (>5 kV), the resulting configuration is limited in capacitance volumetric efficiency (VE) defined as capacitance per unit volume. Multilayer structures are used to optimize VE of high voltage MLC as discussed below.

II. STRUCTURE OF MLC CAPACITORS

Multilayer ceramic capacitors utilize metalized electrode plate structures separated by layers of dielectric ceramic material (Fig. 3). These plate-dielectric structures are arranged in parallel. Capacitances of devices arranged in parallel are additive, therefore, the capacitance in-

creases as the number of active layers increases, per the relationship illustrated in Fig 3.

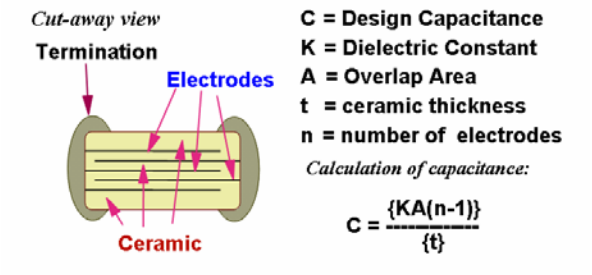

Figure 3. Cutaway view of MLC capacitor.

The co-fired ceramic and metal configuration results in a monolithic chip having the appearance of a solid ceramic block. The multilayer structure enables the use of very thin dielectric layers (today approaching <1 micron), in combination with high layer counts, resulting in relatively high VE capability.

Inside of the monolithic structure, the electrode plates are arranged in a pattern that has adjacent plates extending to opposite faces of the ceramic block, with non-adjacent plates extending to the same face of the block structure in an inter-digitated manner. The exposed electrode edges are electrically interconnected with a common conductor via a metalized coating applied to the exterior opposing faces, called the end termination as indicated in Fig 4.

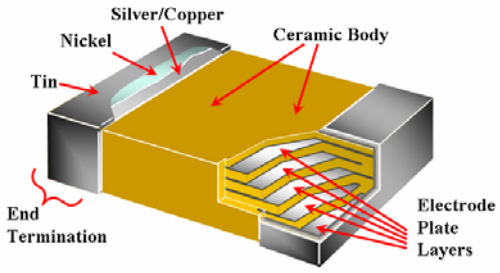

Figure 4. Multilayer ceramic chip structure.

III. THE NON-LINEAR STRESS FACTOR

With lower voltages (<500 VDC), the relationship between voltage stress capability (volts per micron) and dielectric thickness is constant, allowing a linear relationship between dielectric withstanding voltage and dielectric thickness. As shown in Fig. 5, if the applied voltage is doubled (v to $2v$), then doubling the thickness (t to $2t$) creates the same voltage stress.

It would be reasonable to assume that this linear relationship continues with higher voltages and dielectric thicknesses and to achieve very high voltage capability, one only need increase the dielectric proportionately. In reality, that relationship does not hold true for this structure. As shown in Fig. 6, doubling (from $2v$ to $4v$) the voltage capability of the MLC ceramics to voltages beyond 500 VDC, requires increasing the dielectric thickness by a factor of three (from $2t$ to $6t$).

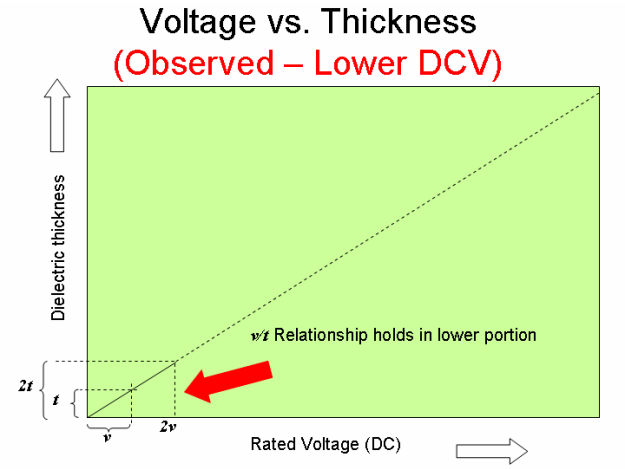

Figure 5. Voltage capability vs. thickness_ low voltage.

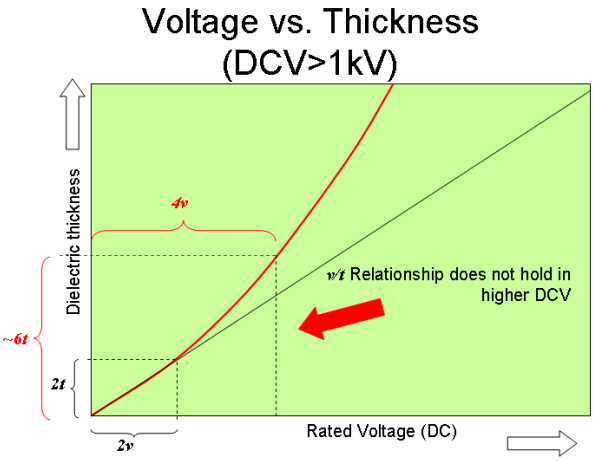

Figure 6. Non-linear relationship: thickness vs. voltage.

Part of this discrepancy may be explained by the complex electric field structures within the MLC under high voltage. The onset of breakdown in a dielectric material will start when the electric field intensity is large enough to begin to tear apart the molecular structure of the material. Electric field intensities near the internal edges of the electrode plate structure are greatly multiplied at high voltage. As indicated in Fig. 7, regions of high electric field extend from the non-terminated edge of the plates to the end margin extensions of the plate. Additional electric field intensity comes from the multilayer structure, as

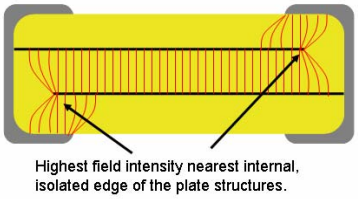

Figure 7. Field concentrations in MLC structure

there are generally plate and end margins above and be-

low each electrode plate. As a result, additional high field fringes are created along the top and bottom faces of the termination wrap.

These field concentrations and the resultant charge disparity at the un-terminated edge of each electrode are illustrated in Fig. 8. The charge is most dense along the un-terminated edge of the electrode because of field fringing effects. In addition, a repulsive effect (common charge) results in maximized charge concentrations at the corners of the electrode edge opposite the termination.

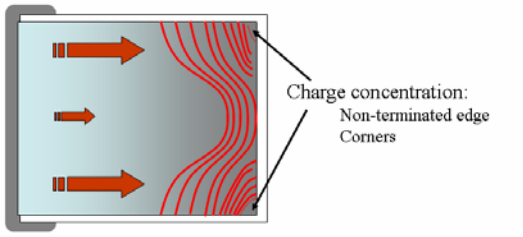

Figure 8. Charge concentration on one plate in MLC.

In order to mitigate the effects of charge concentration in the electrode corners (Fig 9), high voltage plate designs typically utilize radiussed corners [1].

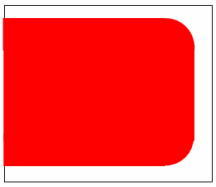

Figure 9. Reducing corner effect with radiussed corners.

IV. DESIGNING IN THE LINEAR PORTION

In order to achieve optimization of dielectric capability, the voltage stress level should be maintained within the linear portion of the voltage thickness relationship (see Figs. 5 and 6). This can be accomplished using a cascaded or floating electrode configuration, wherein the internal electrodes are configured to achieve multiple capacitors in series, which divides the voltage across the cascades. An example of the resulting internal electrode structure is depicted in Fig 10 [2].

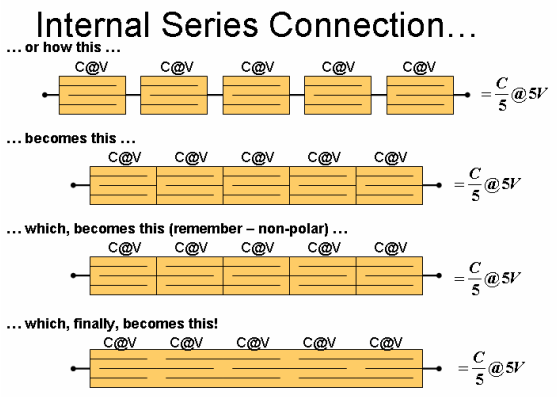

Figure 10. Creating five cascades in one MLC.

In this example, five 1kV capacitors are configured in series. This configuration allows an application of 5kV across the group of five capacitors. Use of a single MLC design having the same number of electrodes, but 5 times the dielectric thickness (*t*) as depicted in Fig. 11, would not work because of the nonlinear relationship illustrated in Fig 6. The voltage capability of the single multilayer device with dielectric thickness of 5*t* would be considerably lower than for the series device.

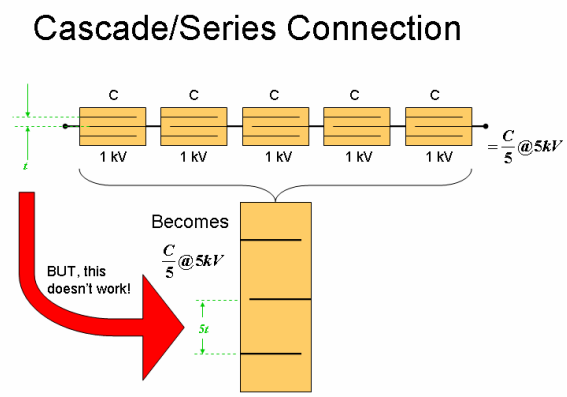

Figure 11. Five cascade vs. one of higher voltage.

Using floating or cascading internal electrode design, the 5 MLCs in series, illustrated in Fig 10, can be accomplished inside of a single MLC. This design configuration maximizes capacitance per unit volume for high voltage capacitor designs (i.e., once the design enters the nonlinear portion of the voltage capability versus dielectric thickness relation in Fig. 6). The 1kV capacitors with capacitance C result in a total capacitance of C/5 when arranged in series configuration. This is equal to the design capacitance of the one, thicker, 5kV capacitor as depicted in Fig. 11.

The internal electrode patterns required for five-cascade, and for four-cascade internal electrode designs respectively are shown in Fig. 12. Cascade designs having an odd number of cascades such as the five-cascade internal electrode design depicted on the left, will exhibit electrode stacking that creates termination contacts for opposite polarities on adjacent electrode planes. Even number cascade designs (such as the four-cascade plate

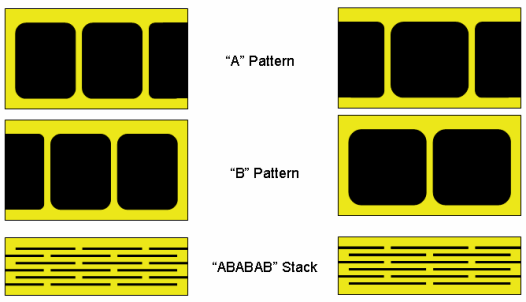

Figure 12. Five and four cascade electrode patterns.

patterns depicted on the right in Fig. 12) have edge contacts for opposite polarity terminations on the same plane. Both of these design configurations yield suitable voltage performance. Note the radius applied to the corners of the overlap portions. The only corners not rounded are those connected to the end termination, as the broadest contact at the termination minimizes ESR (equivalent series resistance) and since these corners do not experience high levels of charge concentration (see Fig. 8), radiusing is not important.

Is this method of cascading efficient? If the voltage versus thickness were to remain linear through these high voltage ranges, then the most efficient design would be achieved with no cascades – a straight thickness for voltage design. The cascade method needs a portion of the volume to establish the non-overlapping plate extensions in between each cascade. Using as few cascades as possible to remain within or near the linear portion of the strain relationship will achieve the highest efficiency.

V. Testing

Because the product is manufactured using high density, monolithic ceramics, they are characterized by the elimination of known failure modes including large voids and delaminations. This characteristic can be established with corona inception and partial discharge testing (per MIL-PRF-49467), familiar to the high voltage community [3,4].

VI. Application Considerations

What advantage does the MLC capacitor bring to high voltage applications? First, the volumetric efficiency over film and mica capacitors is tremendous. Volume declines of 90% have been noted.

Another aspect achievable with the MLC structure is surface mount capability. These chips with ratings from 500 VDC up to 3 kV are in standard EIA chip sizes from 0805 up to 2225, with X7R and C0G dielectric offerings [5]. The dielectric constant of the X7R material are orders of magnitude larger then C0G, film or mica dielectrics allowing capacitance values up to 0.22 uF. The sacrifice for using the X7R is the temperature dependence of capacitance (±15% from -55°C to +125°C), and a negative voltage coefficient.

VII. Summary

The benefits presented with the MLC product offering include volumetric efficiency and surface mount capability. These benefits translate into reduced placement costs, savings in board space, and more uniformed division of voltage across the capacitor. The monolithic structure of this cascade design removes concerns over unequal leakage properties creating a secondary voltage distribution.

Segment	Applications
Power Supply	Input filter, input protection, snubber, high voltage output filter, resonators or tank circuit, invertors, coupling, voltage multipliers, etc.
Industrial/Military	High voltage line filters, blocking, filtering, pulse, ballast, voltage multipliers, etc.
Medical/Automotive	Pulse energy, blocking.

Table 1. Markets and applications for Hi-Voltage MLCs.

These capacitors have pure tin plated external electrodes for good solderability. They are available in case sizes from 0805 to 2225. Dielectrics available are *C0G* and *X7R*.

VIII. References

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