KEMET Electronics Corp.

New Products Being Developed for Flex Crack Reduction and Elimination

There are three restrictions associated with high capacitance multilayer ceramic (MLC) capacitors: the highest capacitance is only available in low voltages; the capacitance is very sensitive to voltage; and, the devices are being developed in smaller case sizes only. These restrictions are the result of creating very thin dielectrics with lower breakdown voltages, the dielectrics are Ferro-electric in nature and the volts per micron strain increases with thinner dielectrics, and the small cases are required to achieve acceptable reliability after surface mount processes.

The number one failure mechanism for MLC capacitors is flex cracking, and by going to larger chips, the incidence of this failure increases. The chart in Figure 1 shows for given failure rates the flexure level for the larger chips is lower than for the smaller chips. This is a matter of physics as the larger chips have a larger span of ceramic between the solder pads. Because of this, these devices are often restricted to the smaller, surface mount packages equal to or smaller than 1510 (3825-mm).

There have been three design modifications offered as a method of reducing the effects of these flex cracks on the capacitor, but in this brief discussion, there is no time to present these other than to list them as: 1. creating thicker cover layers, 2. using larger end margins, and 3. introducing soft, flexible terminations. The first solution seldom works. The third solution, though promising in reducing the incidence of the crack into the ceramic, does not eliminate the crack. The second solution allows the crack to penetrate into a safe region of the structure, and though it can cause a loss of or intermittent capacitance, it eliminates the safety concerns of a "shorted" capacitor appearing in the circuit with large current capability (e.g., battery circuits). None of these solutions allows the designer to begin using larger capacitor packages in his circuit. The remainder of this article discusses solutions that can be applied to 'large' ceramic chips.

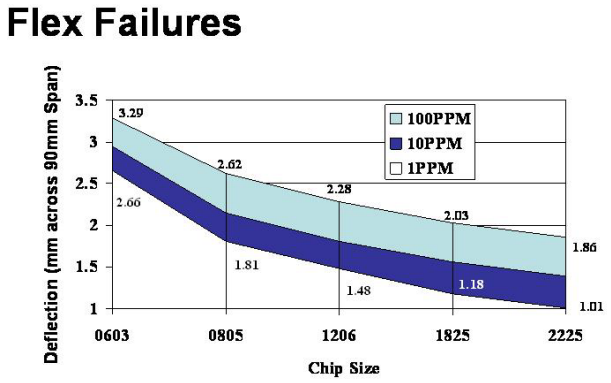

Figure 1. Flexure versus chip size.

One alternate design being pursued by KEMET involves reducing the differences in susceptibility for the larger packages. Remember that the creation of these cracks is related to the span of ceramic between the solder pads. This concept was proven by reducing and extending the terminations on a 1206 (3216-mm) capacitor to create wide versus narrow gaps or separations. Even though the devices were mounted on the same solder pad geometries, the difference is remarkable as the narrow gap parts show a significant increase in flex capability (Figure 2). The number of failures below 2 mm, drops from ten to zero, out of 200 pieces tested in each group.

Extending this concept further, we have proposed a capacitor design with a wrap-under termination that extends towards the middle of the chip, creating a much smaller gap between the terminations, specifically for the larger chips (U.S. Patent

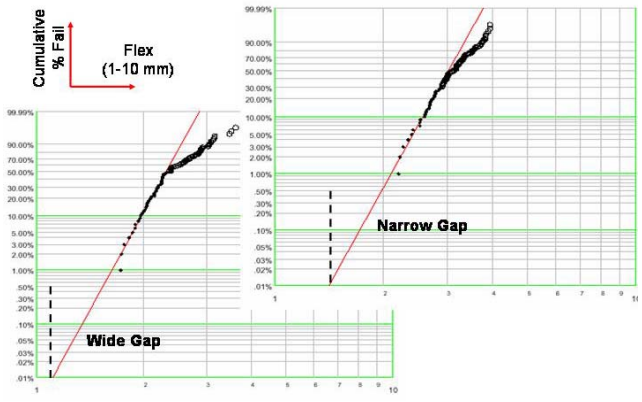

Figure 2. Wide versus narrow ceramic gap between terminations.

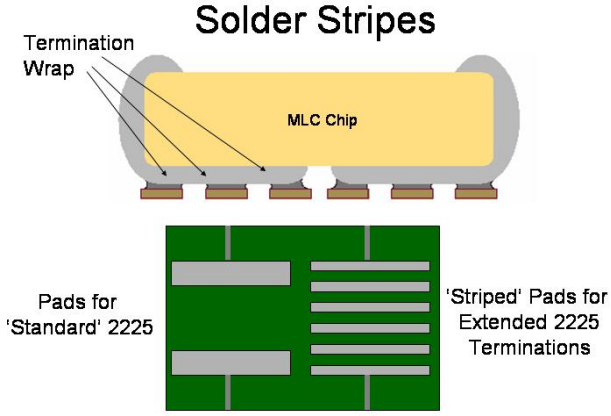

Figure 3. Extended termination wrap-under and striped pads.

No. 6,917,510). These large termination wraps might create problems when the device is mounted to the circuit because of the large mass of solder created; but using a striped termination as shown in Figure 3 alleviates this. We are building 2225 (5664-mm) chip capacitors using the wrap-under design and our expectation is that these devices will have better flex capability than a standard 0603 size chip.

Another variation of this design is to create lands as extensions from the termination and mount solder balls to these extensions. The device would then be a 'flip-chip' or BGA type of capacitor, but cost for this type of process would be prohibitive.

The second alternative design is intended to eliminate these cracks from ever appearing in the device. History has shown that a leadframe connection between the ceramic chip and the circuit board eliminates these cracks but introduces additional problems such as mechanical susceptibility to shock or vibration, handling, and cost. The leadframe requires a free vertical element to prevent any mechanical forces generated at the solder pads from creating a parallel force in the ceramic. This vertical element as shown in Figure 4 must be long enough to prevent the under-wrap of the termination from ever contacting the solder pad, or wicking solder along the leadframe to create a hard mechanical connection here.

This vertical element created a 'stand-off' between the board and the capacitor that eliminates mechanical force transitions, but adds to the electrical path (resistance and inductance are added) and the thermal path (power dissipation is reduced).

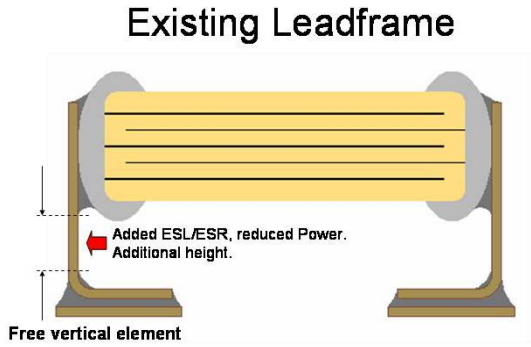

Figure 4. Old style leadframe eliminates flex cracks because of free vertical element.

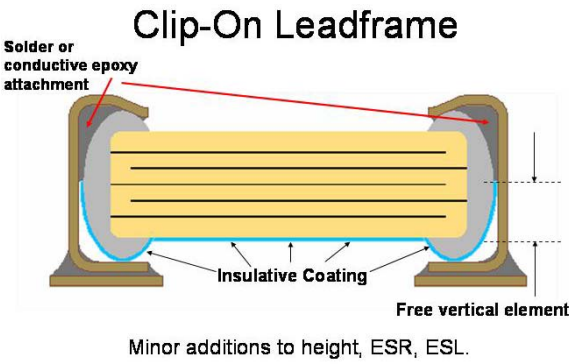

Figure 5. Clip-on leadframe eliminates flex cracks - regardless of chip size.

In Figure 5, we have reduced the standoff for a leadframe attachment to nearly zero, while still maintaining a free vertical element of the leadframe. In this concept (U.S. Patent No. 6,903,920), a thin insulative, non-solderable film is applied to the lower surface of the capacitor, prior to the attachment of the leadframe. The leadframe is applied to achieve electrical and mechanical contact along the upper regions of the termination faces. The film prevents the solder from forming a mechanical contact at the bottom of the chip, and the free vertical element is achieved in the film-covered region of the capacitor. Comparing this approach with the old style leadframe, it greatly reduces the center of gravity, the added resistive and inductive elements, as well as achieves a much shorter thermal path.

Both of these concepts are targeted for larger ceramic chip sizes. Though these chips may take up more real estate, an alternative utilization could be to mount the devices vertically, if chip height could be tolerated more than board area. In this case, an additional stabilization would have to be added if the environment included severe shock or vibration exposures. We are in the process of gathering data on the capability of these concepts across several designs, and we will publish that when it is available.

John Prymak – Applications Manager/USA
Ken Lai – Technical Sales Coordinator/Taiwan