

Product Update – Ceramic Fail-Open for Flex-Cracks

The ceramic chip capacitor is generally considered one of the most reliable capacitor types. Typical breakdown voltages are anywhere from 6 to 30 times the rated voltages. The failure of one of these devices is usually preceded by the creation of a defect within the monolithic package while the device is being mounted on the PCB or at some point after the mount. The ceramic material within this device is extremely hard and brittle, with poor thermal transfer capabilities and poor mechanical strain capabilities.

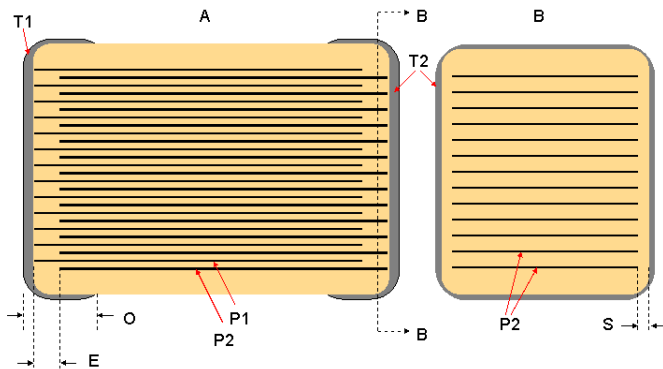


Figure 1. Ceramic MLC structure.

MLC Structure

The structure of a ceramic capacitor is shown in Figure 1. The capacitor consists of layers of ceramic dielectric and metal electrodes. Consecutive metal layers (P1 and P2) are terminated on opposite ends of the chip (T1 and T2, respectively). Repeating this alternating arrangement up through the stack results in a parallel connection of many capacitors.

The unterminated edges of the plates are separated from the opposite termination face by an end-margin (E) and the terminations wrap around the adjacent faces by an overlap margin (O). In order to maximize the volumetric efficiency of the capacitor, the electrodes' end margins (E) and side margins (S) are maintained to as small a distance as feasible. It is therefore 'normal' for the overlap (O) to be considerably larger than the end-margin (E). It is the extension (O) which accounts for the length of the termination pad's contact face, and this length and pad dimension is defined by the EIA.

The termination (T1 and T2) material is usually a copper or silver dominated base with glass frit mixed in to create a mechanical bond to the ceramic block. These terminations are subsequently plated with a nickel overcoat to prevent leaching of the termination base metal into the solder during

the solder reflow process. The nickel is then plated with tin to facilitate wetting of the chip with solder.

Thermal Gradients – Thermal Shock

The ceramic element within this structure is the backbone that defines the shape and rigidity of this device. The electrode plate elements that penetrate into the ceramic block offer a much greater thermal conductivity than the ceramic itself. During the solder heating, finite-element analysis shows the terminations and electrodes quickly transfer and conduct heat into the depths of the ceramic structure, where it then radiates into the adjacent ceramic material itself. The ceramic, as a poorer thermal conductor, allows thermal gradients to be created within the ceramic as the distance from the metal contacts increase. If the rate of heat transfer is too rapid, then the thermal gradients become steeper and the ceramic can tear itself apart as one region is heating and expanding (controlled by its thermal coefficient of expansion or TCE) while regions in close proximity are not as hot. A physical shear force is created within the ceramic structure.

Because the transfer from plate into the ceramic separating the electrodes is critical and forces developed here are focused within the electrode to ceramic boundary, the signature of the thermal cracked ceramic chip is a crack that extends within this interface, outward through the side margins. The crack may extend along the side of the chip, from termination to termination, as if a fracture of the ceramic layer was activated, as it is.

This crack can either be created by having the rate of temperature change well above the recommended 4°C/sec temperature change, in the ramp phases of the solder process, or can be triggered by a structural defect. Any anomalous object caught within electrode to ceramic barrier can intensify the thermal gradient leading to a point-of-failure and strict clean-room conditions are enforced to reduce these possibilities.

Strain and Flex

Once the ceramic chip is bonded to the board with the solder process, the chip is rigidly attached to the surface of the board. Immediately after the solder process, the chip is held in a compressive state as during the cool-down, the board (epoxy-glass type) shrinks more than the chip. This is because the TCE of the chip is lower than that of the board. This compressive nature is alleviated with time as the malleable solder displaces itself to achieve a non-stressful connection between the chip and board.

If the chip is initially at a non-stressful state, then bending the board from beneath and upward creates a shear force - the

greater the bend, the greater the force. Although ceramic capacitors have a high tolerance for compressive forces, their capabilities for shear forces are very weak. This mechanical crack (Figure 2) always starts at the end of the termination wrap under the chip and extends upward. The face of the chip in contact with the termination wrap under the chip is held rigidly along the length of this contact to the board.

Flex Crack

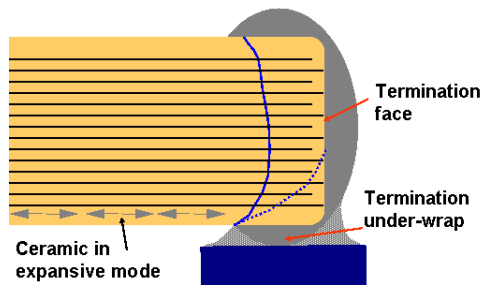


Figure 2. Flex cracks in MLC.

With a shear force developed, the ceramic suspended between these contacts is in an expansive mode, and the elasticity of ceramic is nearly non-existent. The region between the rigidly fixed ceramic and the suspended ceramic in expansion, create tensors focusing the forces at the ends of the under wrap, until a crack is created. This type of crack is referred to as a flex crack. It can travel nearly vertical, up into the top overlap region or at an angle into the termination face of the chip. As the ceramic chip size increases, the susceptibility to flex cracking also increases.

When the crack extends up into the region of the capacitor where electrode plates from both terminations exist, the potential for electrical failure exists. Detection is nearly impossible for visual inspection as the crack is hidden below the surface of the termination. The crack in itself is not a high conductive path until ionics and moisture can penetrate into the crevice. Capacitance, DF, ESR, and even leakage measurements are unable to detect this fresh crack. It can happen only after the chip capacitor is soldered to the board, and it can happen any time after that. Unsupported boards pressured by keypads, buttons and cable connections can develop this flex crack at the end users' site.

The application of the bend force is not the only method of creating this crack. If the board is heated rapidly from the face opposite the side of the chip termination, the board could be put into an expansion mode, which again creates this shear force at the bottom of the chip, and creating the same mechanical crack (thermally created mechanical displacement). In addition, bending the board in the opposite direction will create highly compressive forces that can displace the malleable solder. Once the solder is displaced and the board is allowed to return to its original state, a shear force is now created, raising the possibility for flex cracking to occur.

Short Manifestation

Once the crack is created, it may not be readily detected electrically. A small DC voltage may not create sufficient stress to create a runaway state of increasing current within a short time. In the case of the flex crack, the crack can exist in a nonconductive state for a long time after creation. With time, temperature cycles, moisture exposure and increased stress levels, the crack can grow an ionic path that at first becomes noticeably leaky, then quickly deteriorates into a highly conductive path within the ceramic dielectric. The time to failure is unpredictable, and can occur in minutes, hours, days, months, and longer.

The "Burning" Ceramic

Ceramic does not burn, but consider the following scenario:

- A fault begins to draw increasing leakage current.
- The heat within this finite path and the electrode contacts increases rapidly.
- The heat creates a steep thermal gradient within the ceramic structure.
- The thermal gradient creates more cracks radiating outward (spider cracks) from the initial site, fracturing more ceramic, creating more fault sites.
- The heat is sufficient to melt the electrode, and the ionic current now pulls the metallic compound within the fractured ceramic.
- As long as the current continues, the fracturing and metallic mixture continues with a mass of suspended ceramic particles mixed within a liquidous metallic ball.
- The current flows through multiple, fine paths defined by the metal dispersed within the fractured ceramic.
- The resistivity of these multiple paths is sufficient to keep the mixture in a state of plasma, or a very high temperature mass suspended between the termination pads.
- The temperature (>1600°C) is in excess of the combustion temperatures of the glass-epoxy boards.
- The plasma burns the board beneath it, until the combustion of the board forces a break in the plasma or gravity allows the device to drop off the board, eventually opening the circuit.

There are many alternatives possible with the above scenario. Once the board starts to burn, the power planes within the board could divert the current away from the plasma so now the current starts to burn an increasing number of traces within the board. There are many more possibilities present once the failure begins to collapse within the ceramic chip.

Associated Hazards

The ceramic with the metal strands in the plasma state, cannot achieve temperatures to vaporize the ceramic base structures. It may be possible to achieve temperatures sufficient to melt the metals (>1600°C). Of more importance is the burning of the board. With the many possible material variations of the board structure plus coatings, the epoxy ma-

materials may be the key in defining any gasses evolved from this event.

Flex related – Fail-Open Capacitors

A new line of “fail-open” capacitors can greatly reduce the possibilities associated with the burning board scenario. It should be pointed out that these “fail-open” capacitors should be labeled as “flex related - fail-open” capacitors because a fault within the electrode overlap areas of the capacitor can still evolve into the burning board scenario, but that the design of these pieces are targeted at eliminating the fault source as flex type of cracks.

The approach that KEMET is utilizing in their product offering is to create safe regions in the capacitor (Figure 3) where a flex crack cannot pass through oppositely terminated electrodes. The flex crack always begins at the extreme edge of the termination under-wrap, along the bottom surface of the chip, and then travels upward towards the top face, or towards the termination face.

The fail-open design removes any opposing electrodes from this end-margin area susceptible to the flex crack, excluding the overlap region from that area in between these end-margin areas. The crack potential still exists, but the crack will only penetrate through plates of the same potential. Though this could lead to “open,” high DF, high ESR, or intermittent impedances, it will not allow any current concentrations leading to the burning board scenarios. The sacrifice

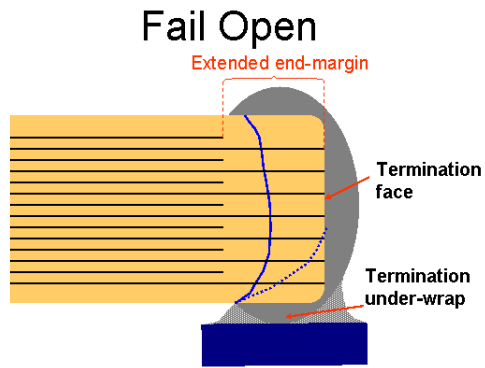


Figure 3. Flex-crack / fail-open design.

paid for this design for a specific capacitance, voltage, and dielectric, is that there are more layers required for the fail-open design, leading to more material and more assembly time.

This fail-open solution addresses the dominating cause for ceramic capacitor cracking which can lead to catastrophic failures. It does not address the thermal cracking mentioned earlier, nor does it address impact cracks, or failures due to anomalous structural defects, and electrical overstress failures.

John D. Prymak
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July 7, 2004¹

¹ Replaces Product Update – “Ceramic Catastrophic Failure Sequence Leading to Hot Shorts,” May 2003, KEMET Electronics Corp.